

Applicant(s): Patrizio Vinciarelli

FACTORIZED POWER ARCHITECTURE WITH POINT OF  
LOAD SINE AMPLITUDE CONVERTERS

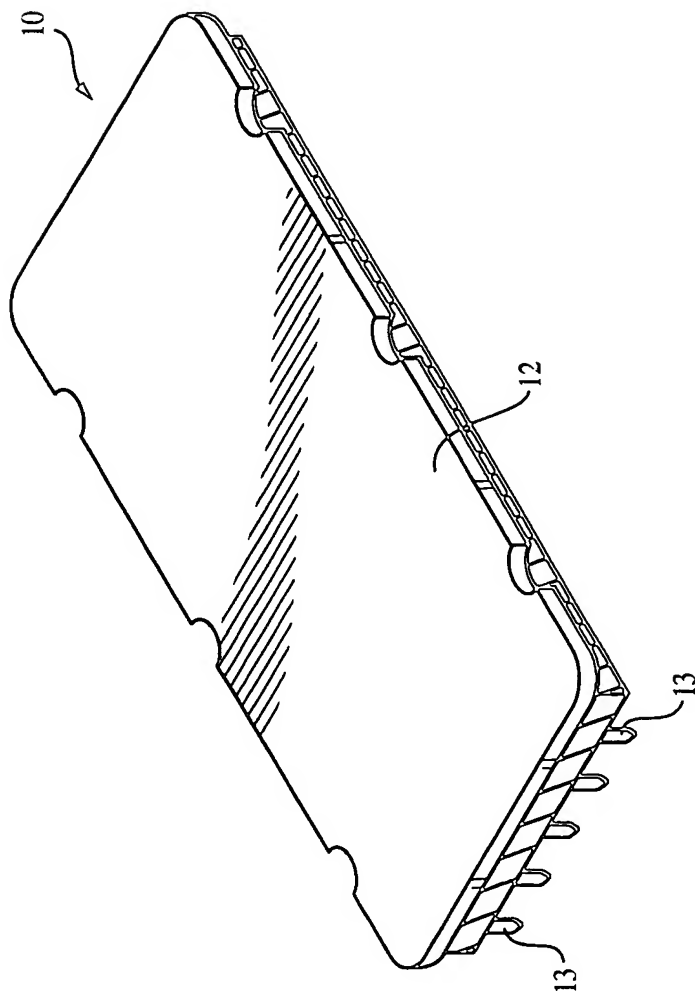


FIG. 1

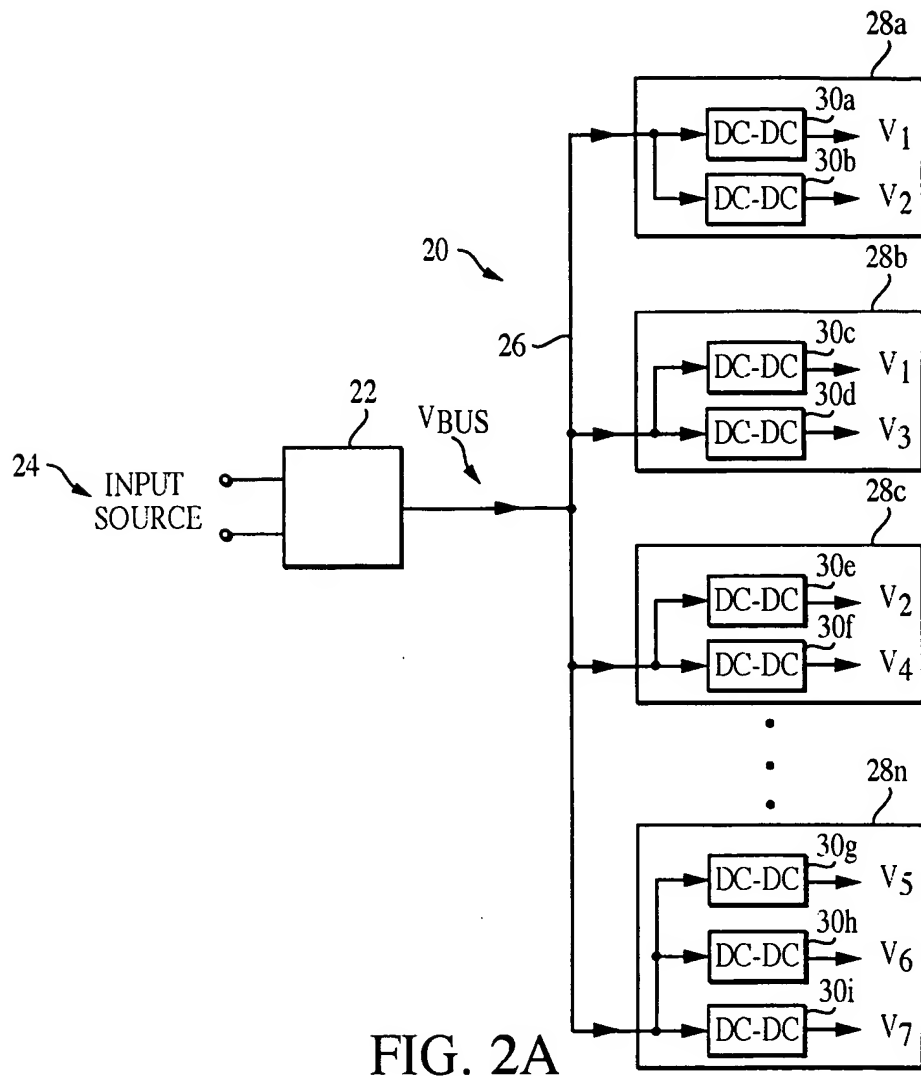


FIG. 2A

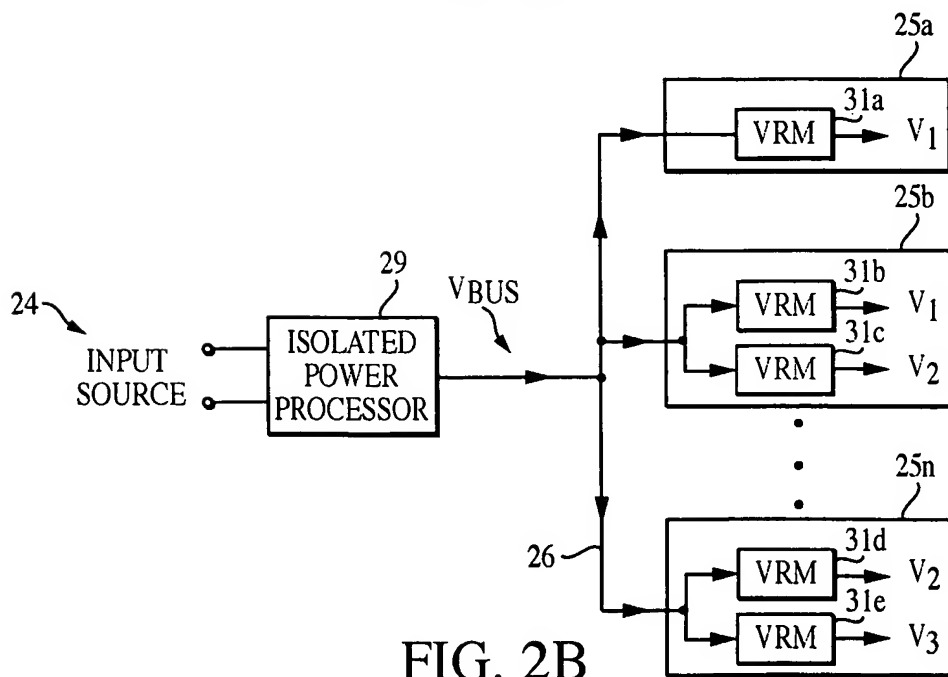


FIG. 2B

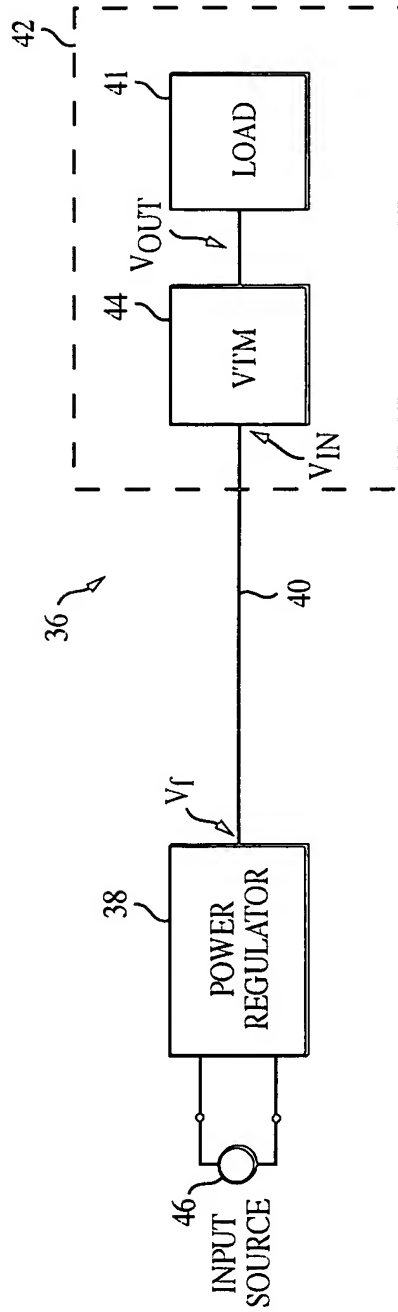


FIG. 3A

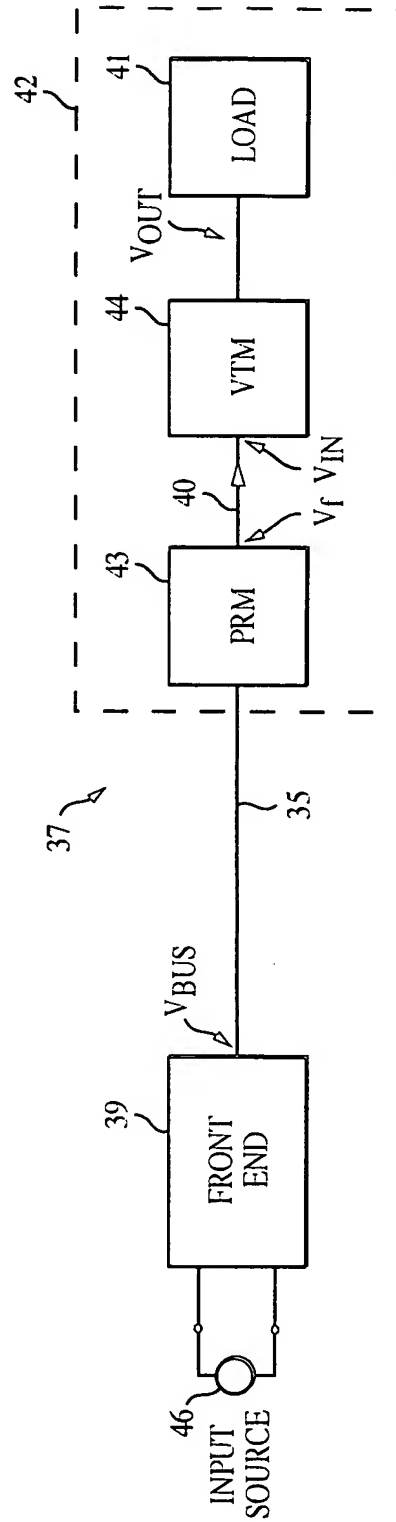


FIG. 3B

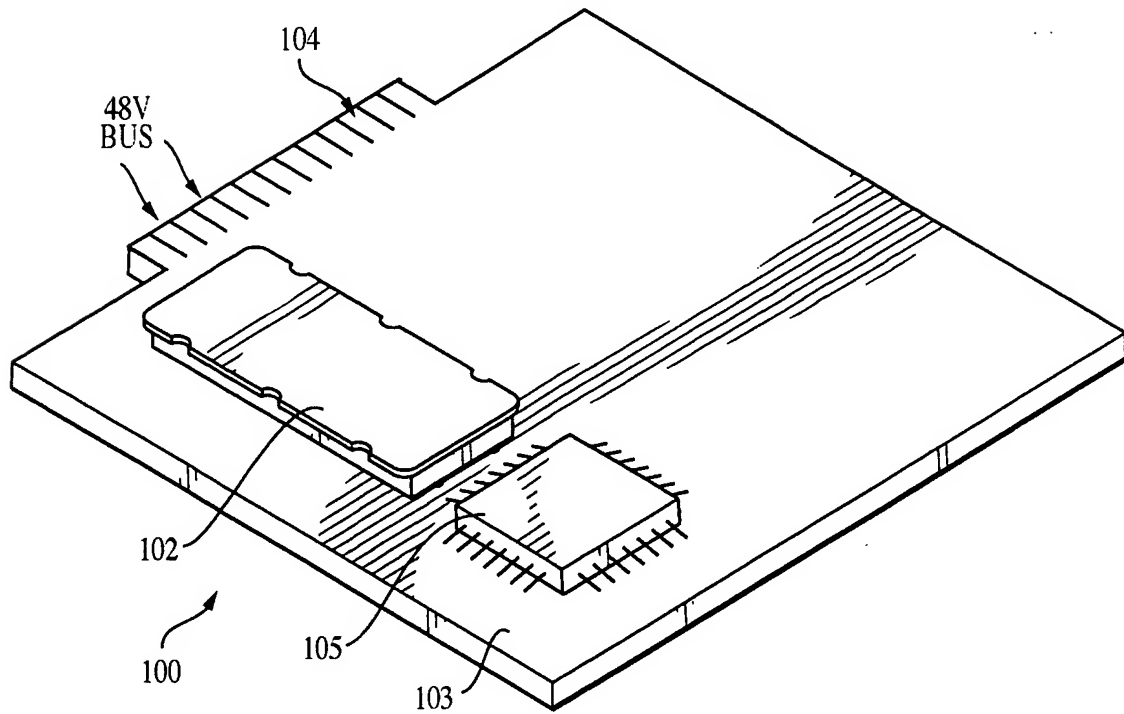


FIG. 4A

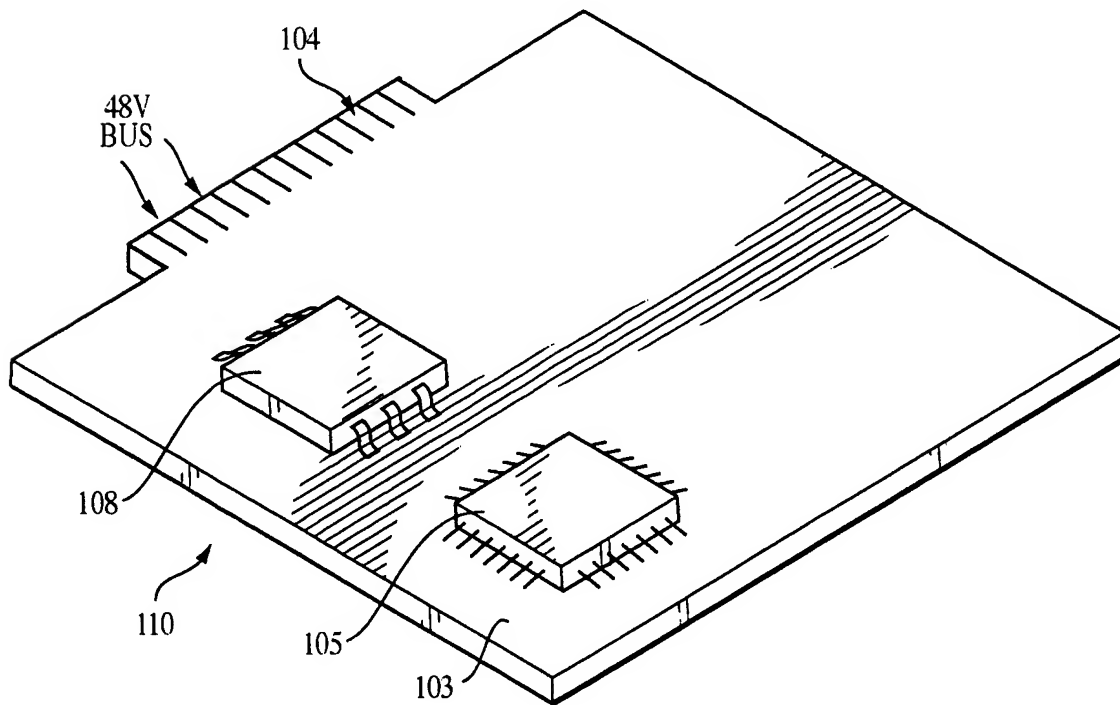


FIG. 4B

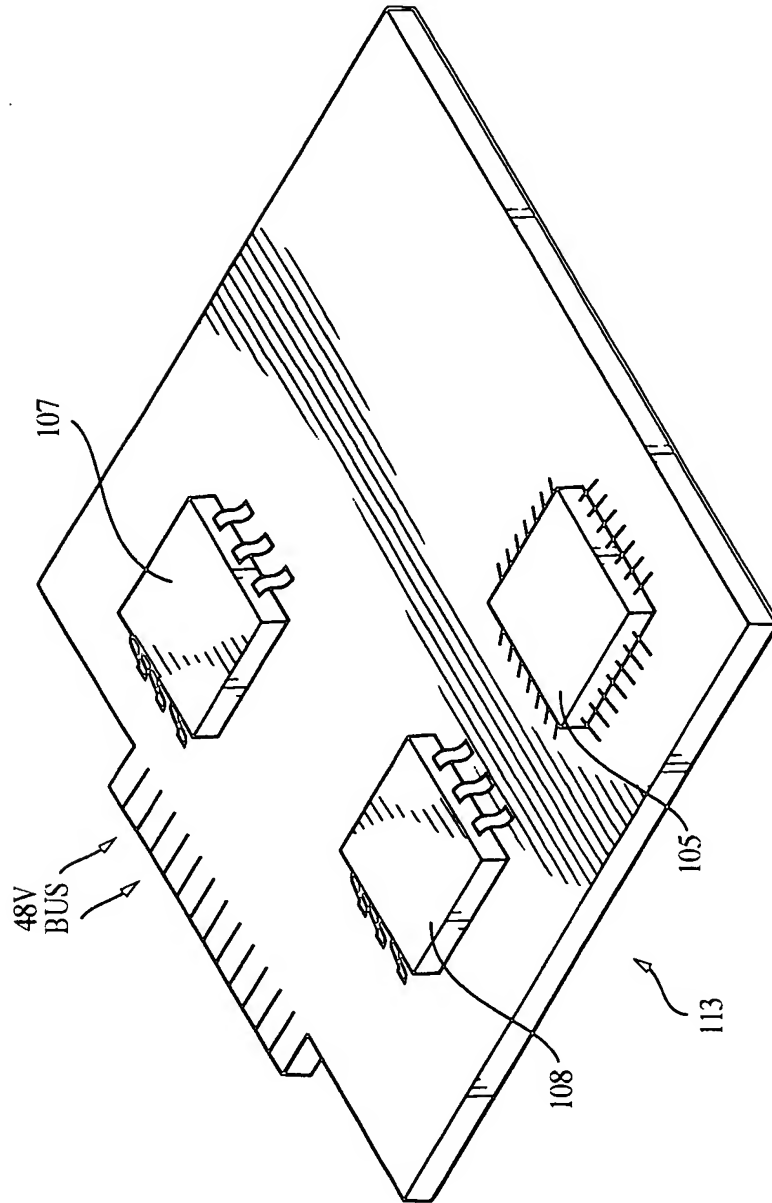


FIG. 4C

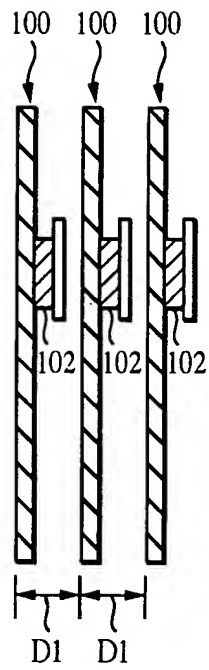


FIG. 5A

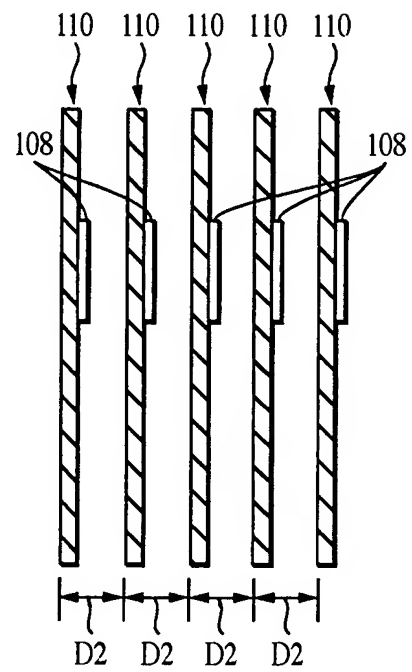


FIG. 5B

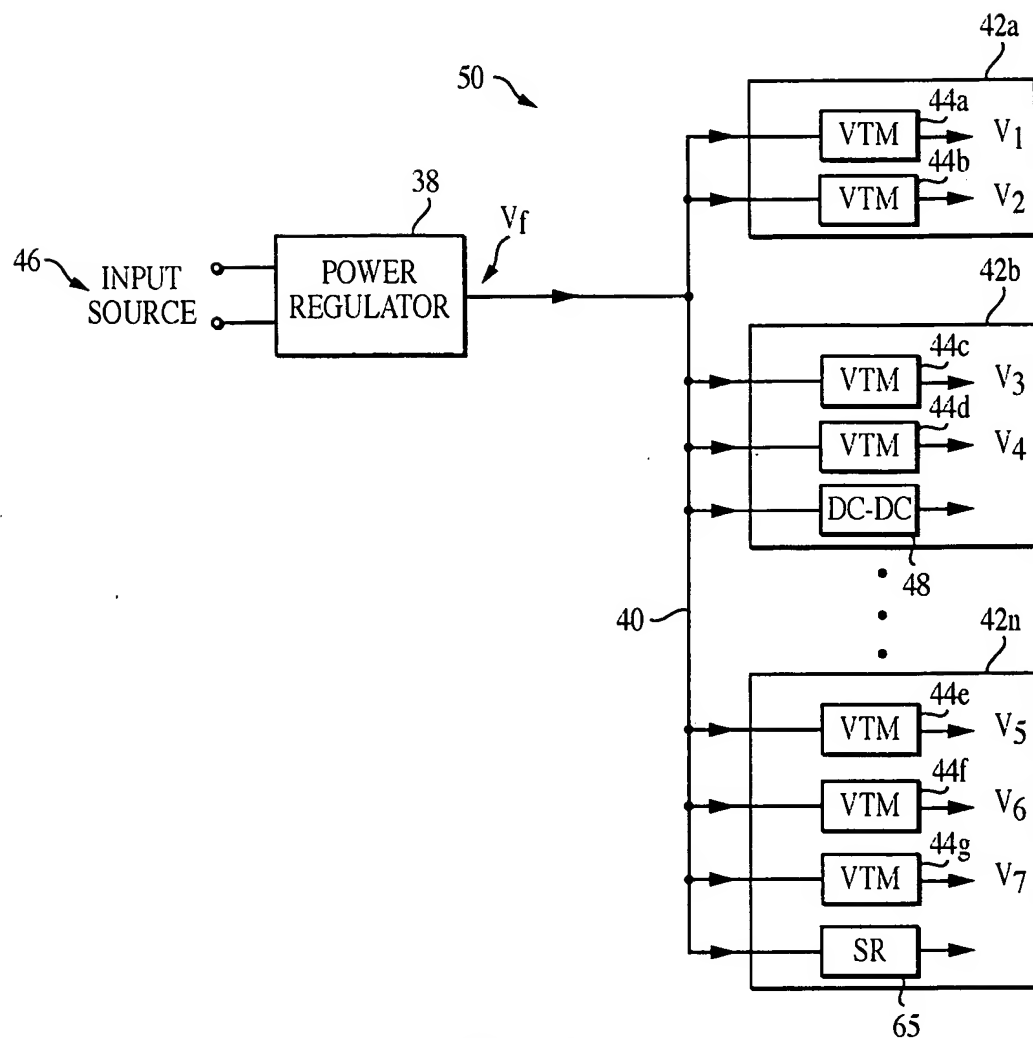


FIG. 6

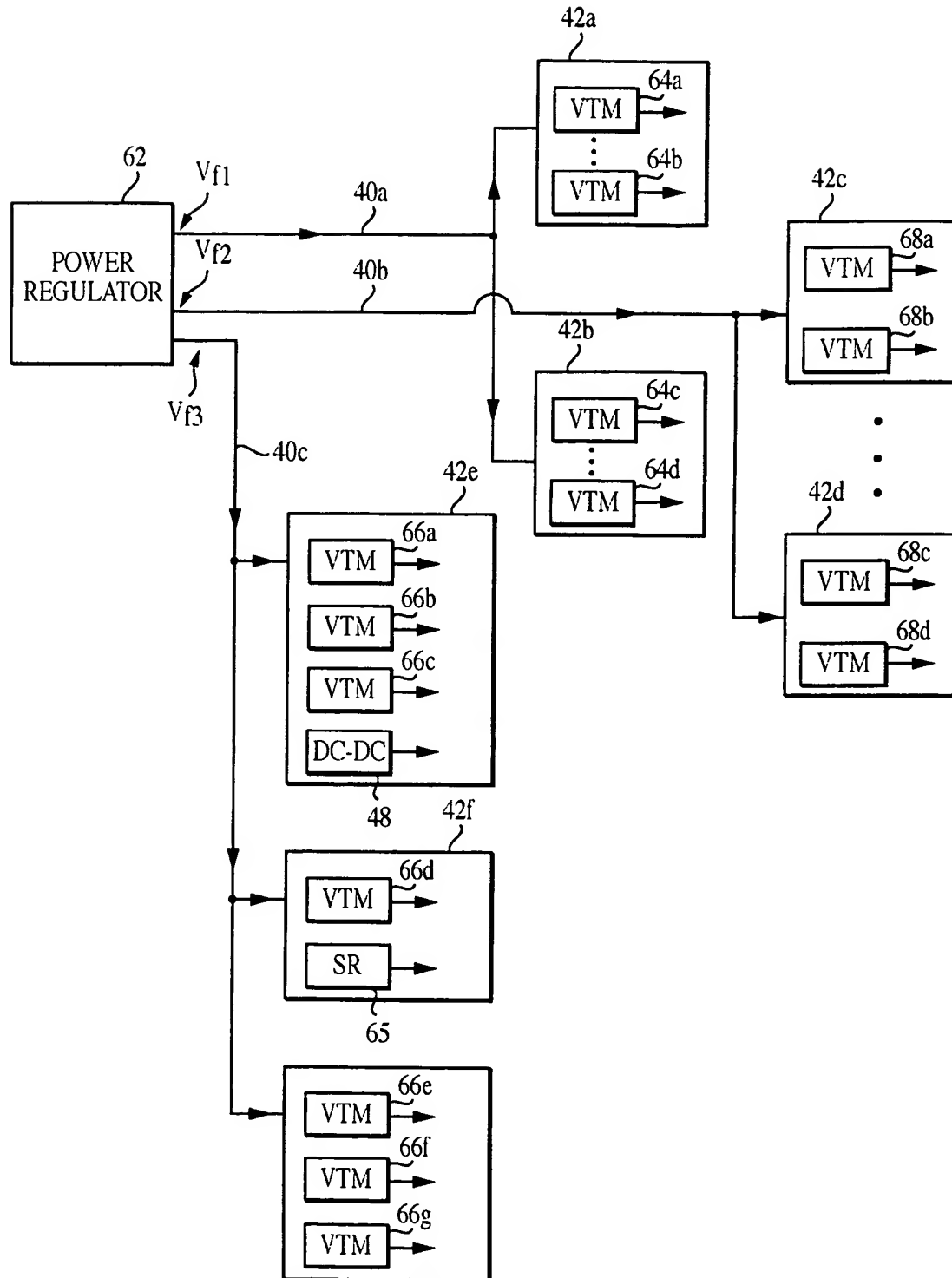


FIG. 7



FIG. 8A

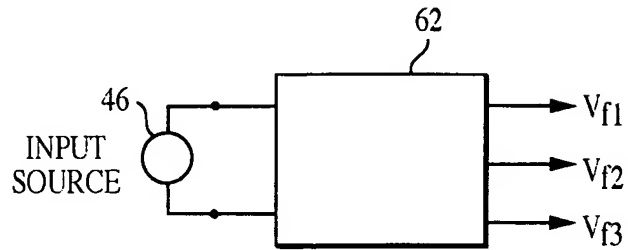


FIG. 8B

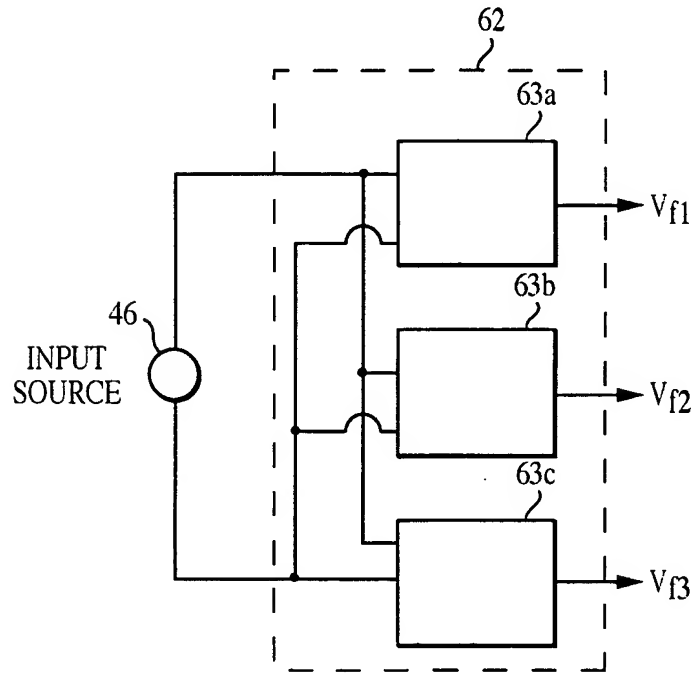
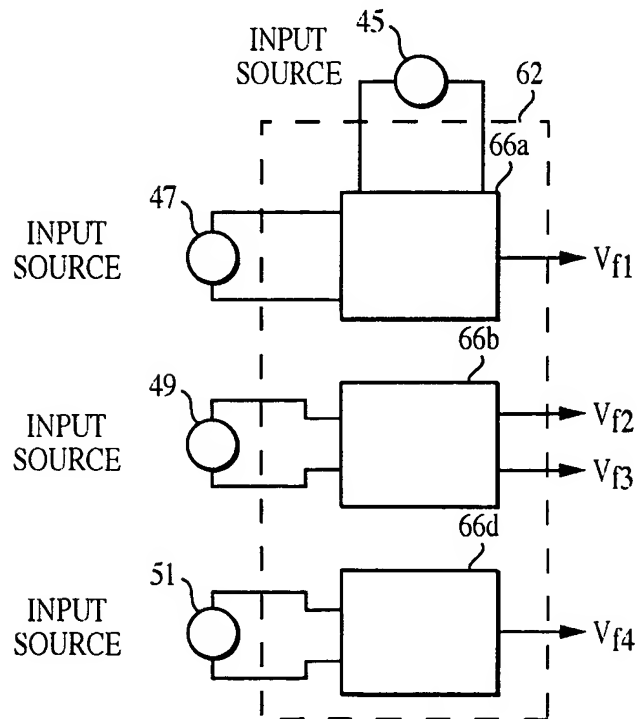


FIG. 8C



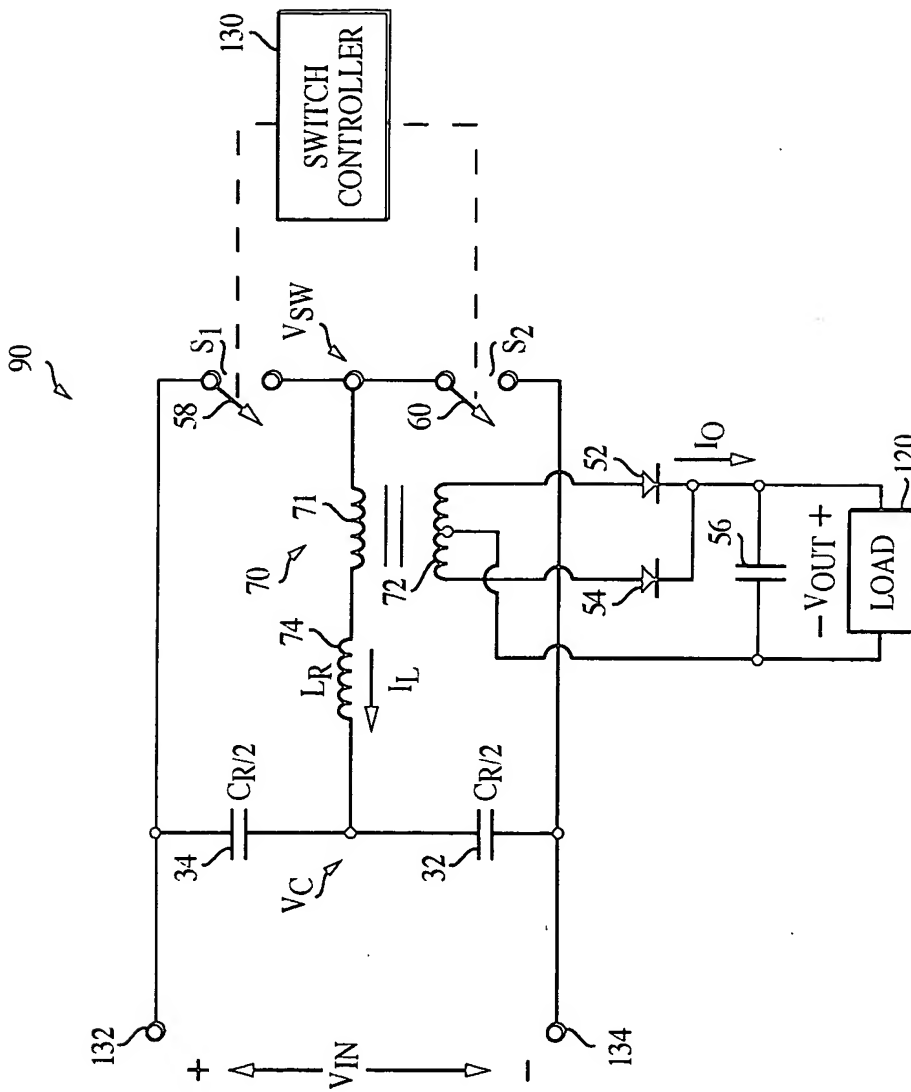
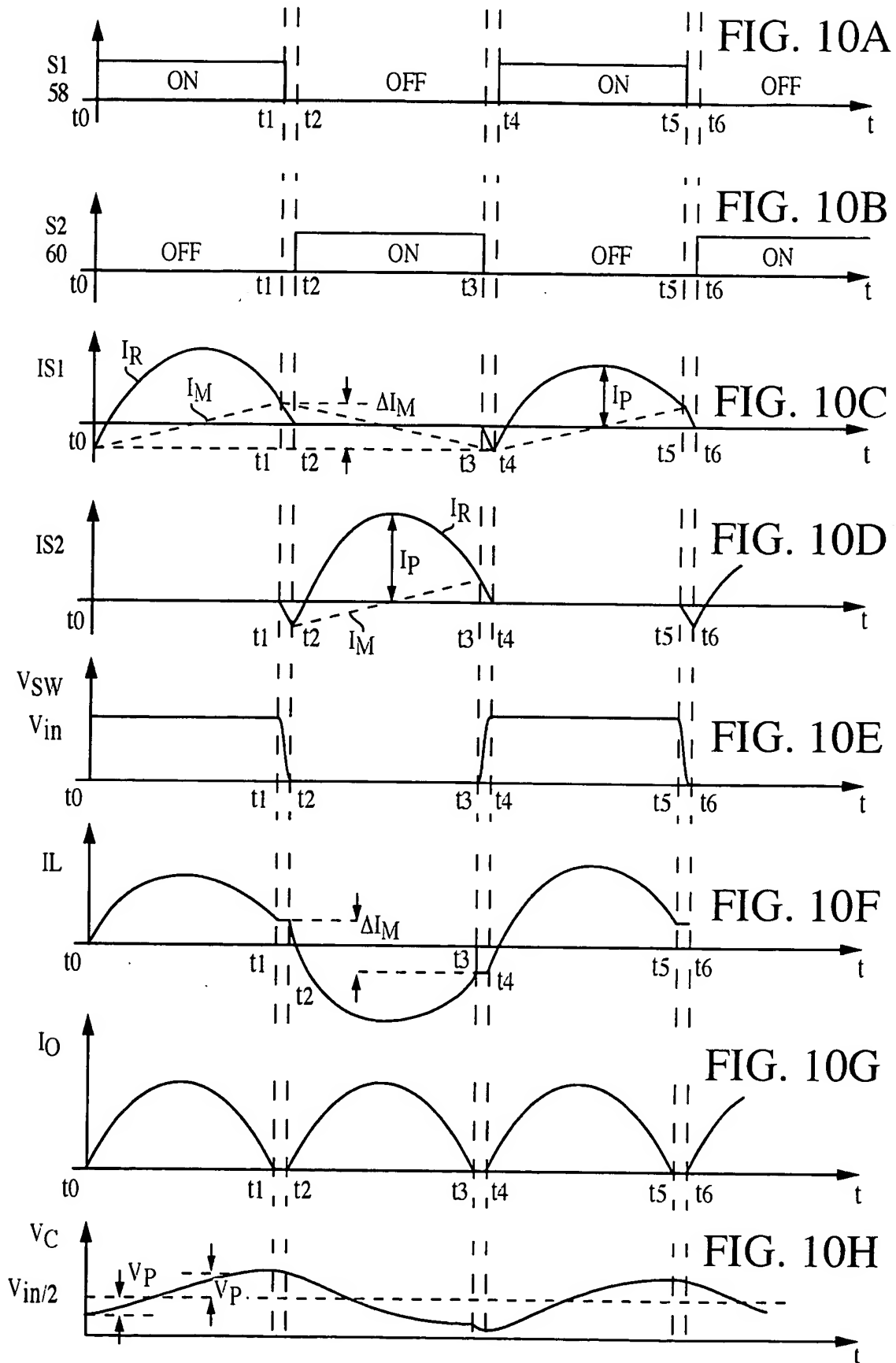


FIG. 9



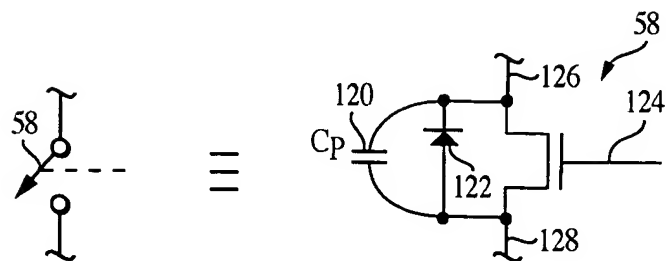


FIG. 11

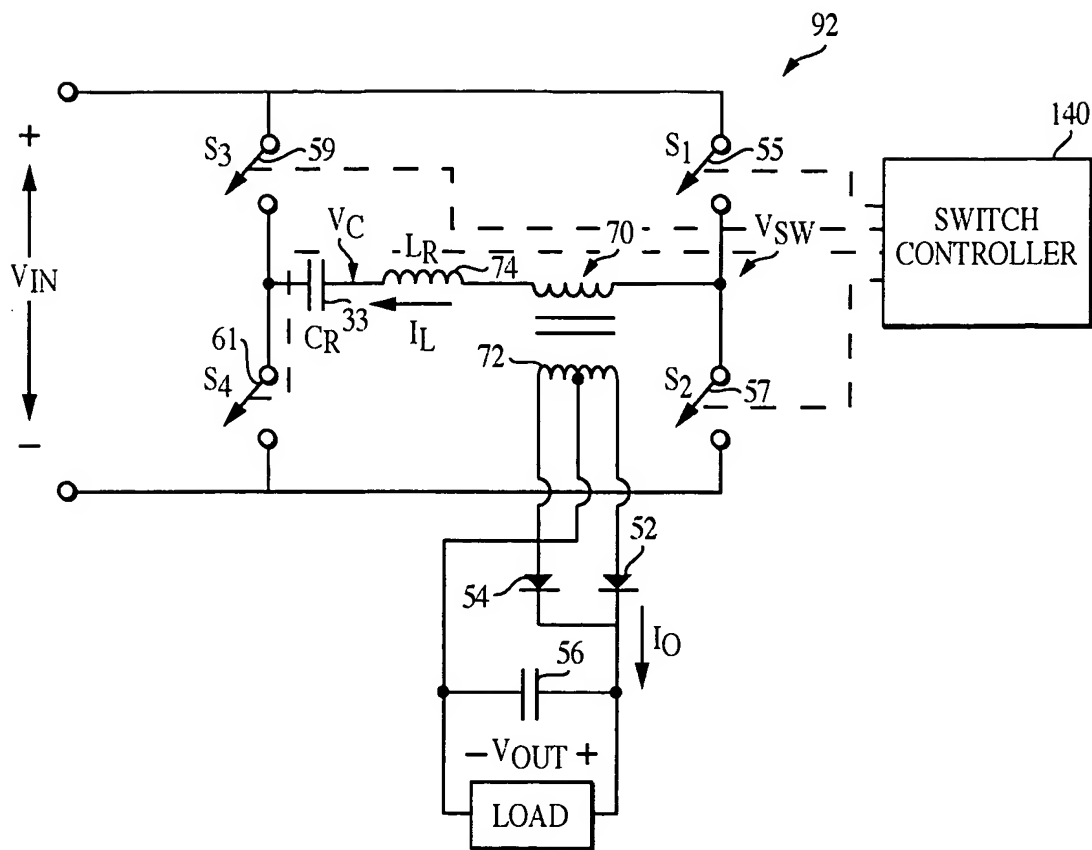


FIG. 12

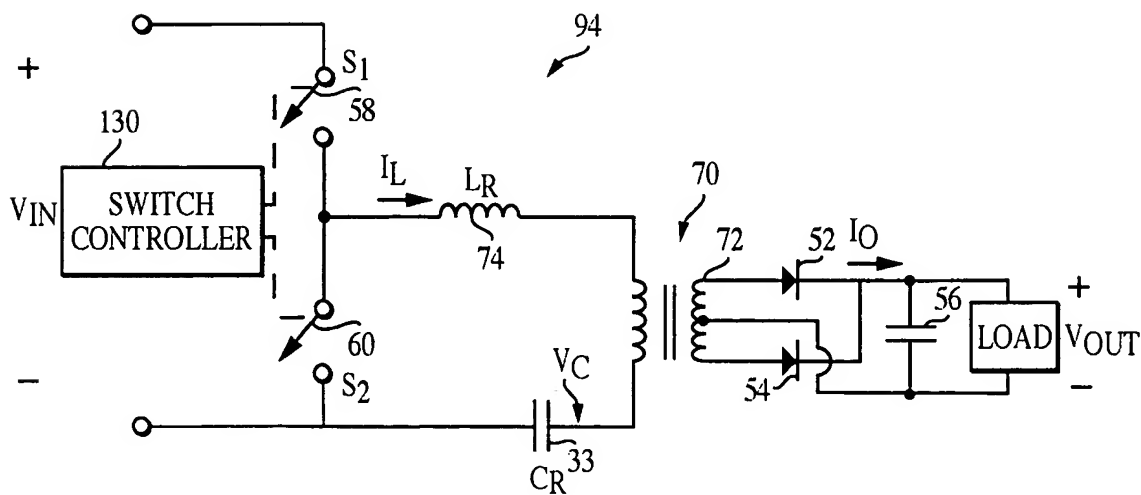


FIG. 13

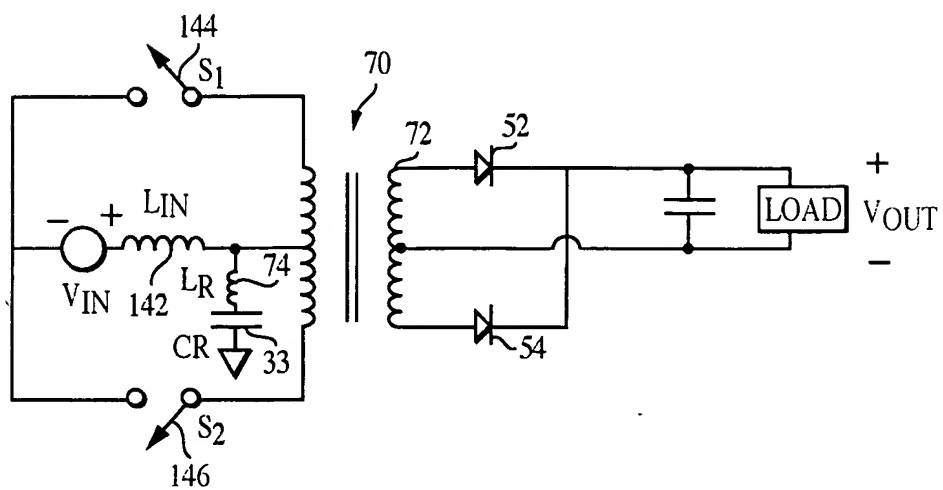


FIG. 14

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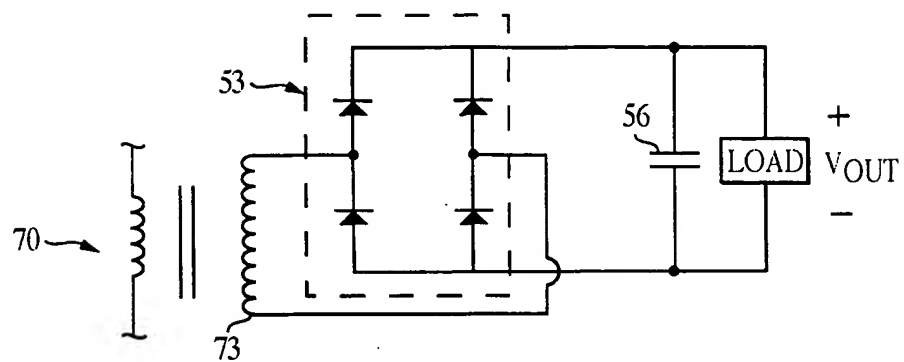
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FIG. 15A

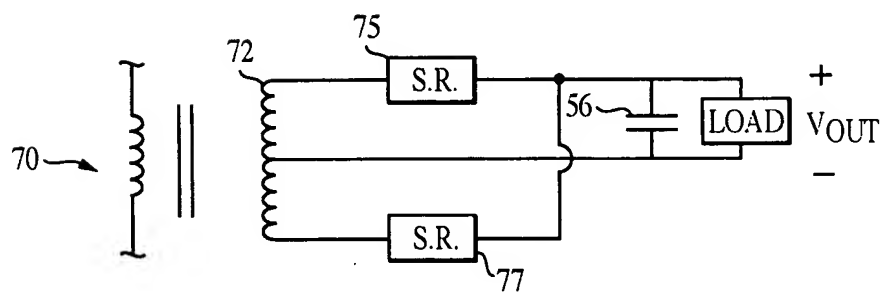


FIG. 15B

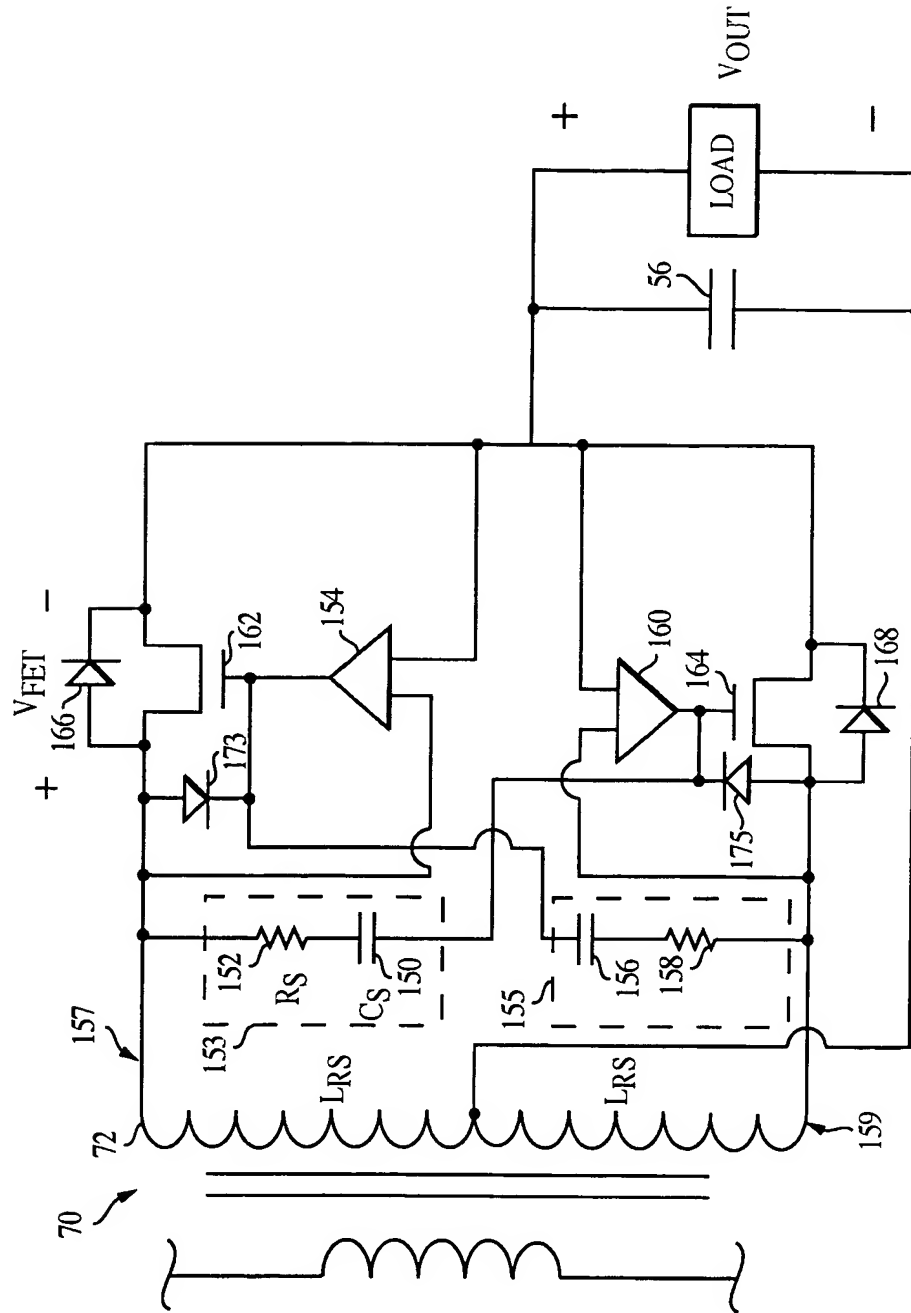


FIG. 15C



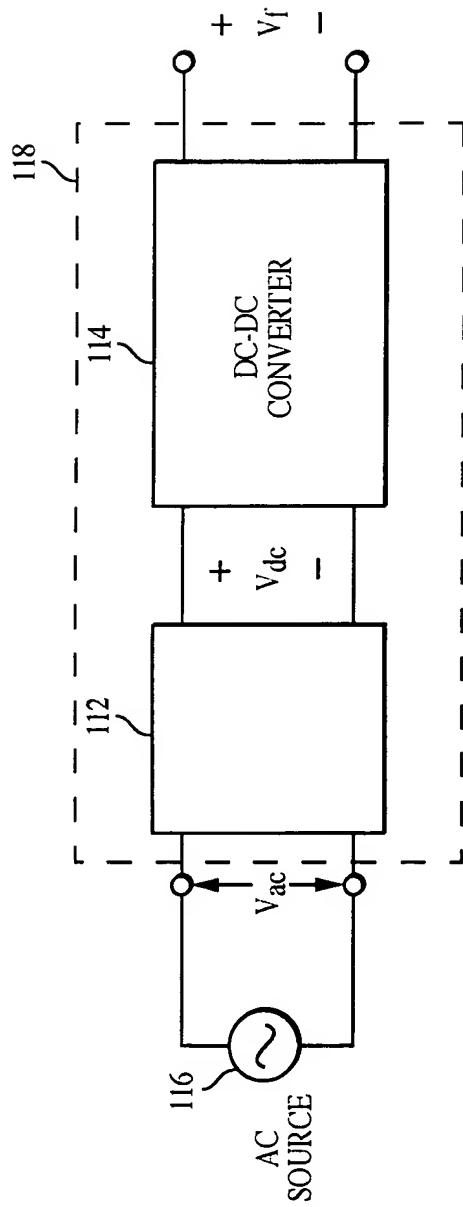


FIG. 16

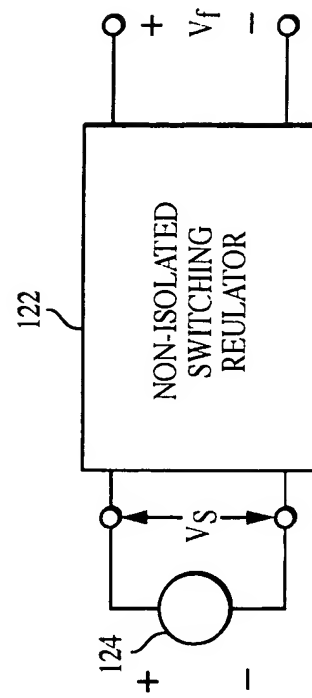


FIG. 17

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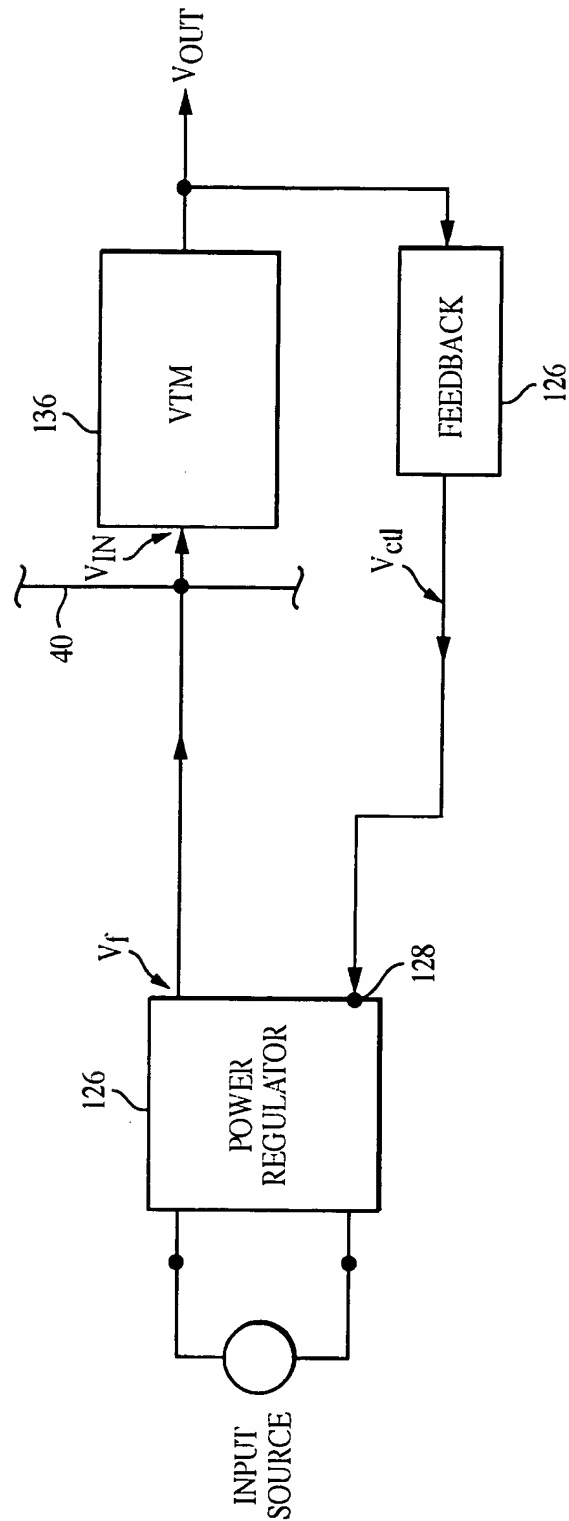
FACTORIZED POWER ARCHITECTURE WITH POINT OF  
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FIG. 18

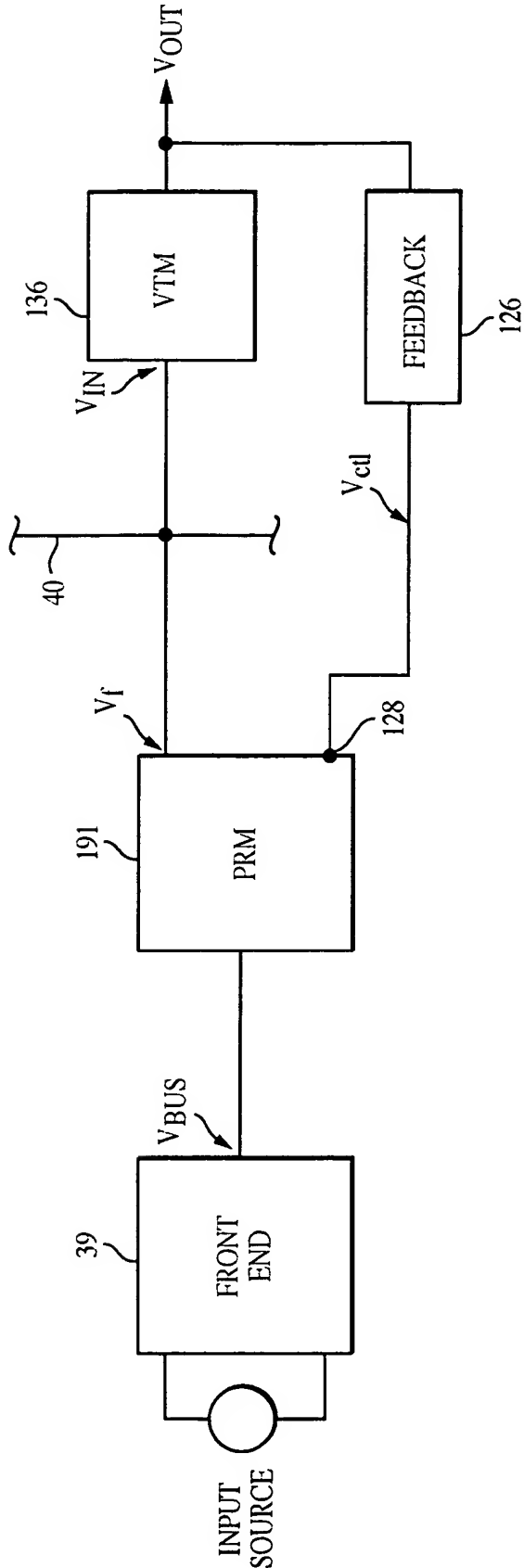


FIG. 19

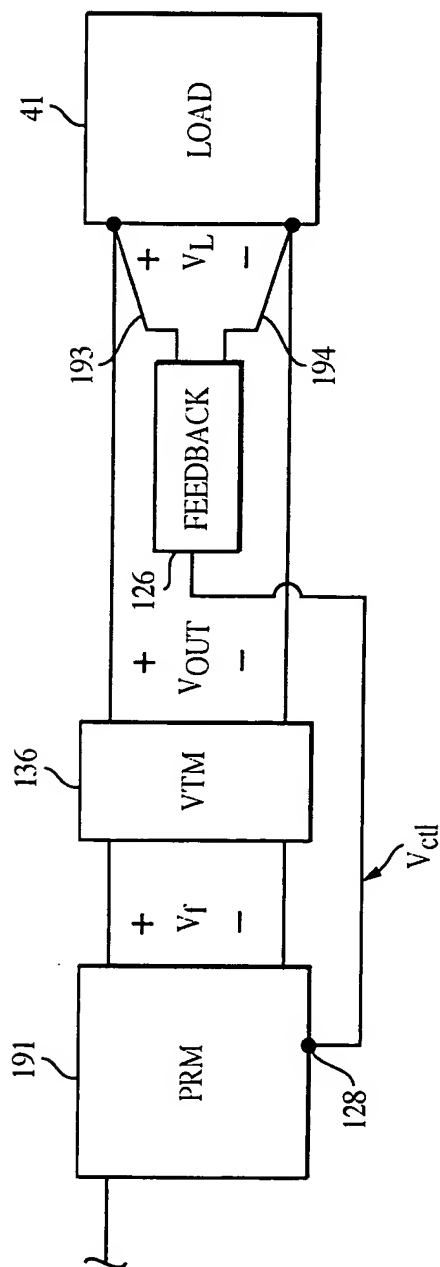


FIG. 20

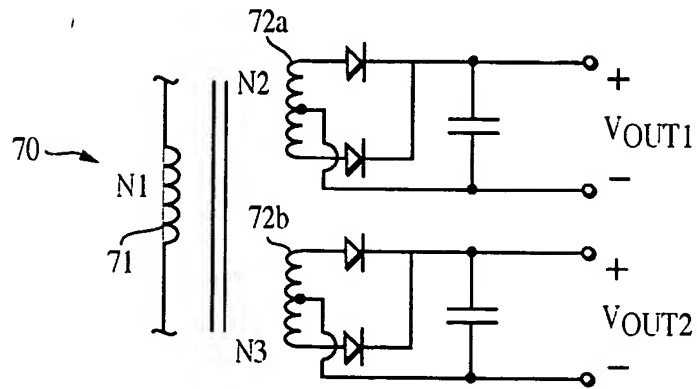


FIG. 21

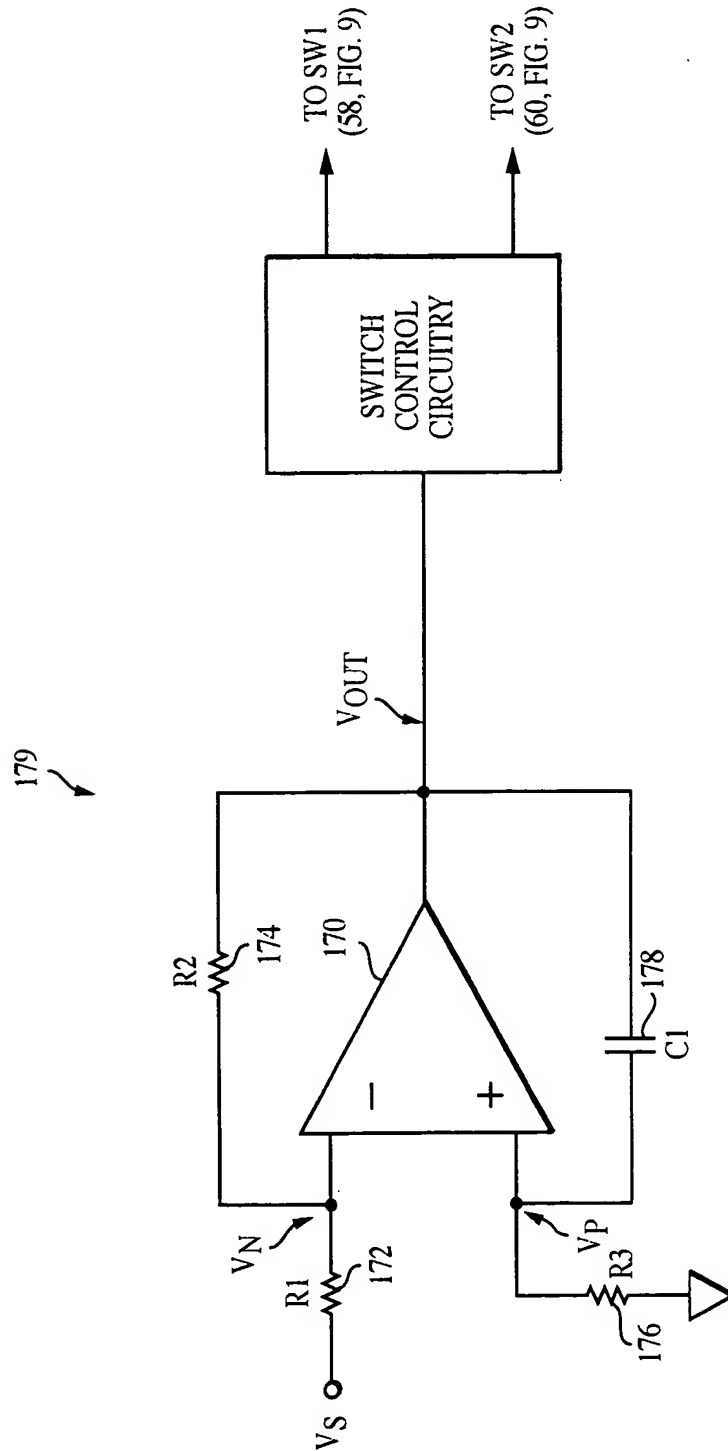
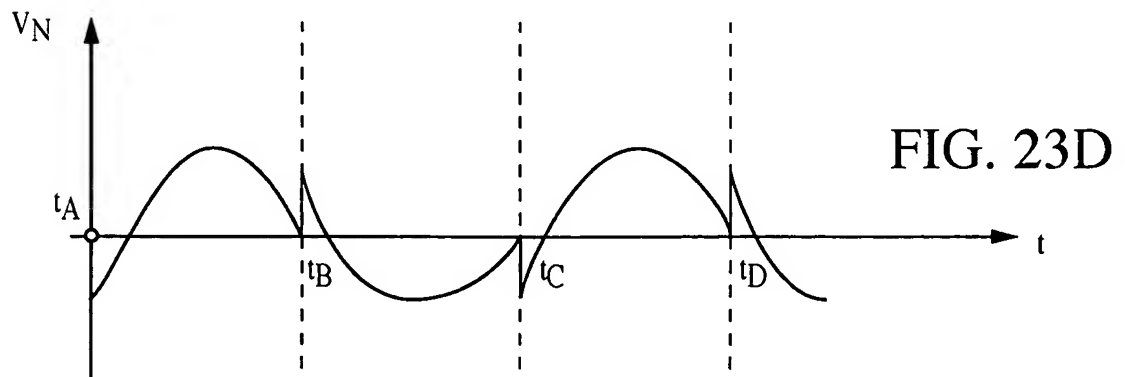
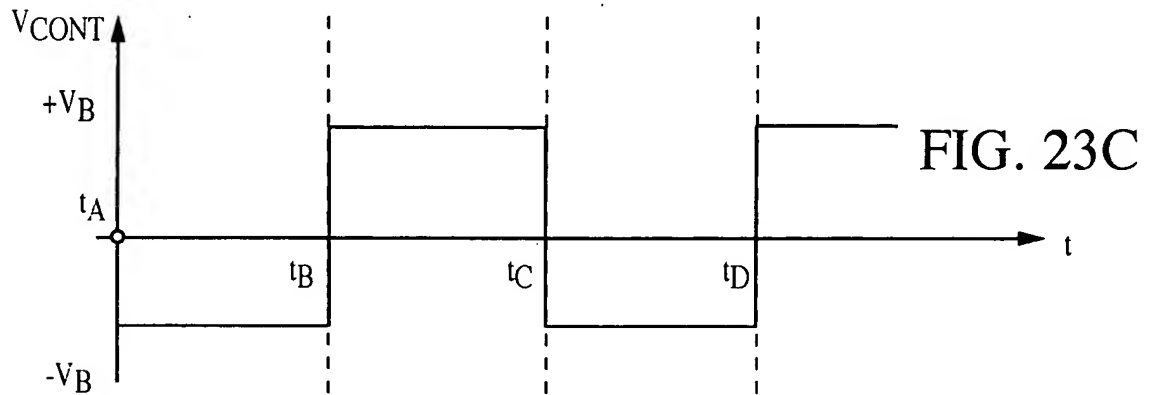
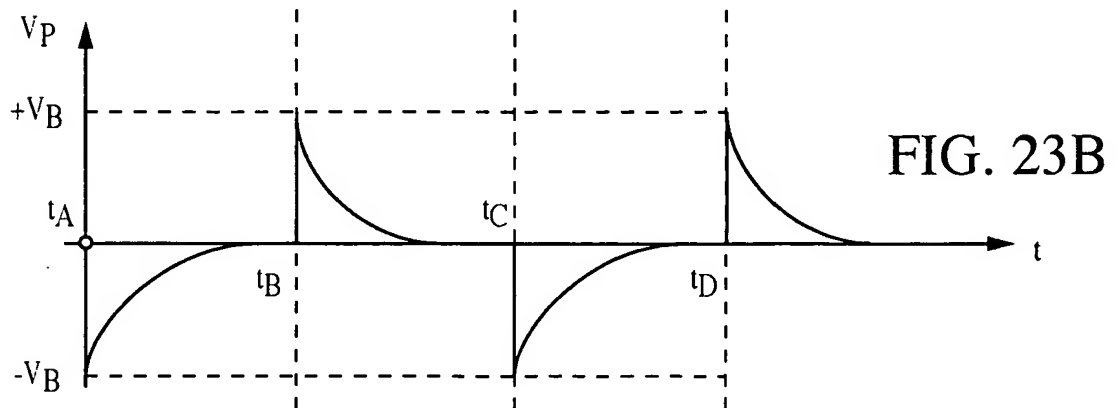
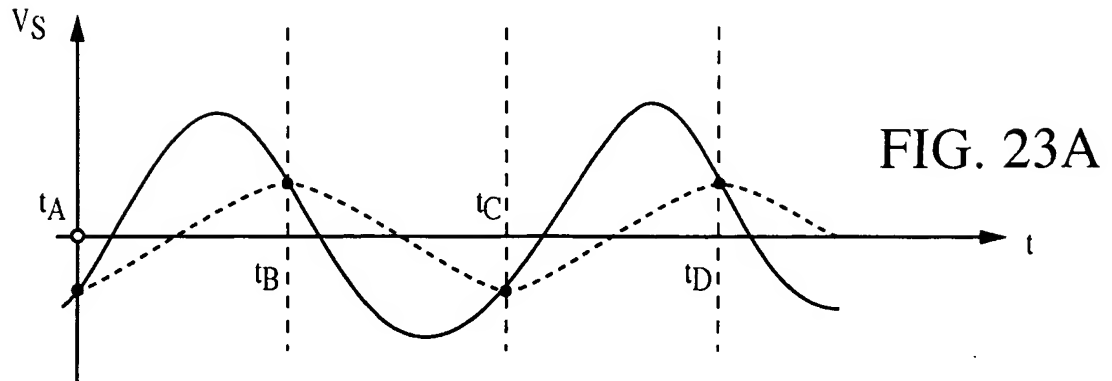


FIG. 22



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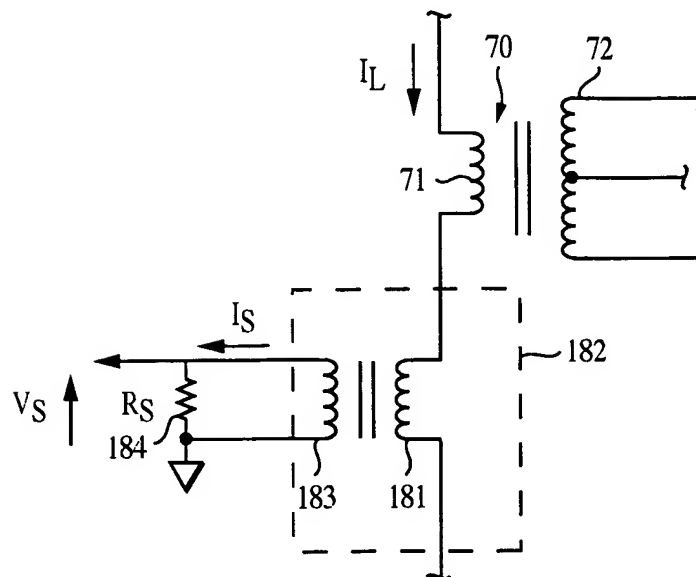
FACTORIZED POWER ARCHITECTURE WITH POINT OF  
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FIG. 24



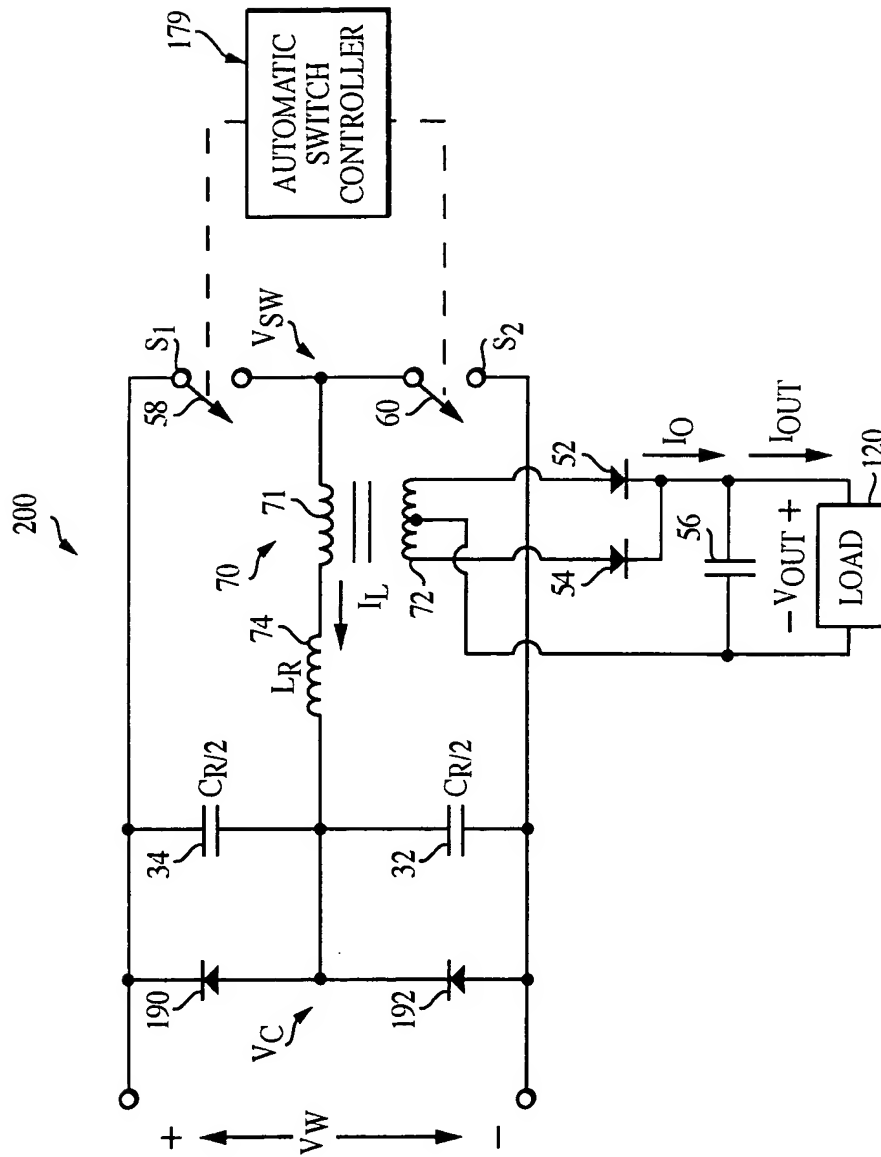


FIG. 25

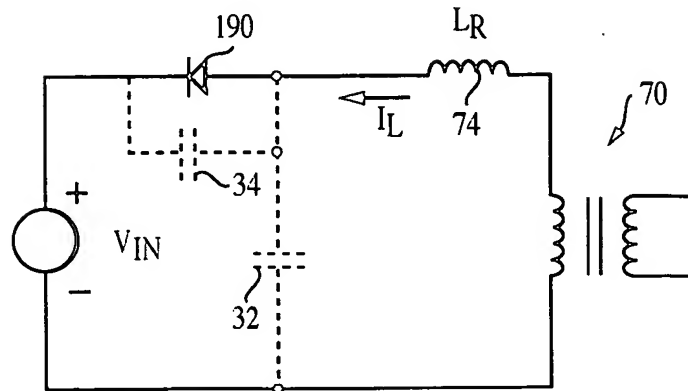


FIG. 26

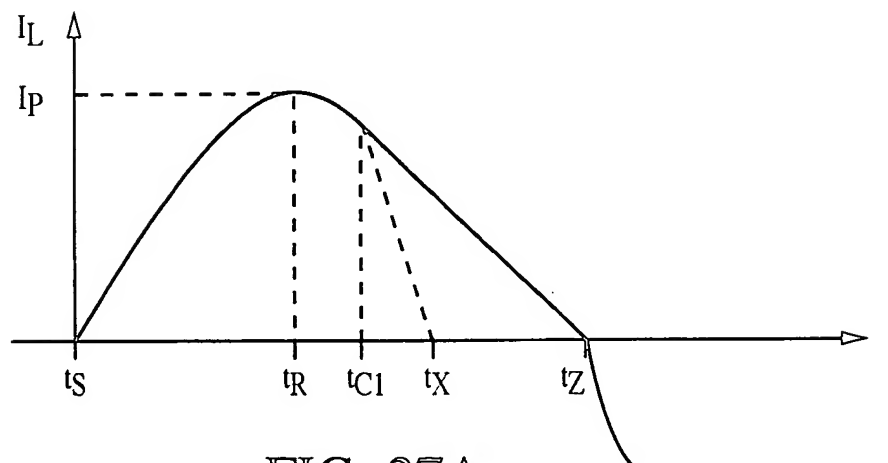


FIG. 27A

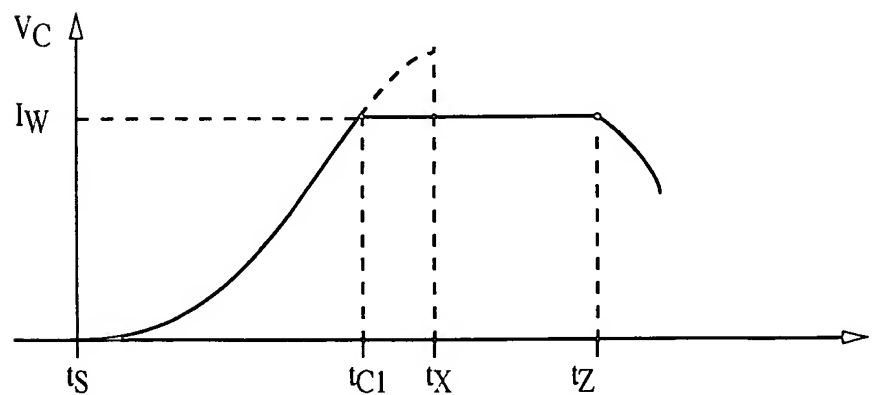


FIG. 27B

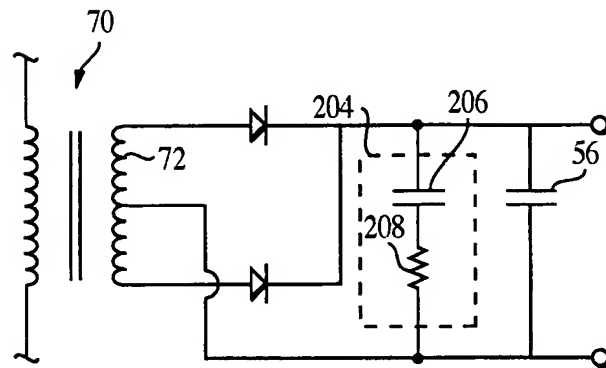


FIG. 28

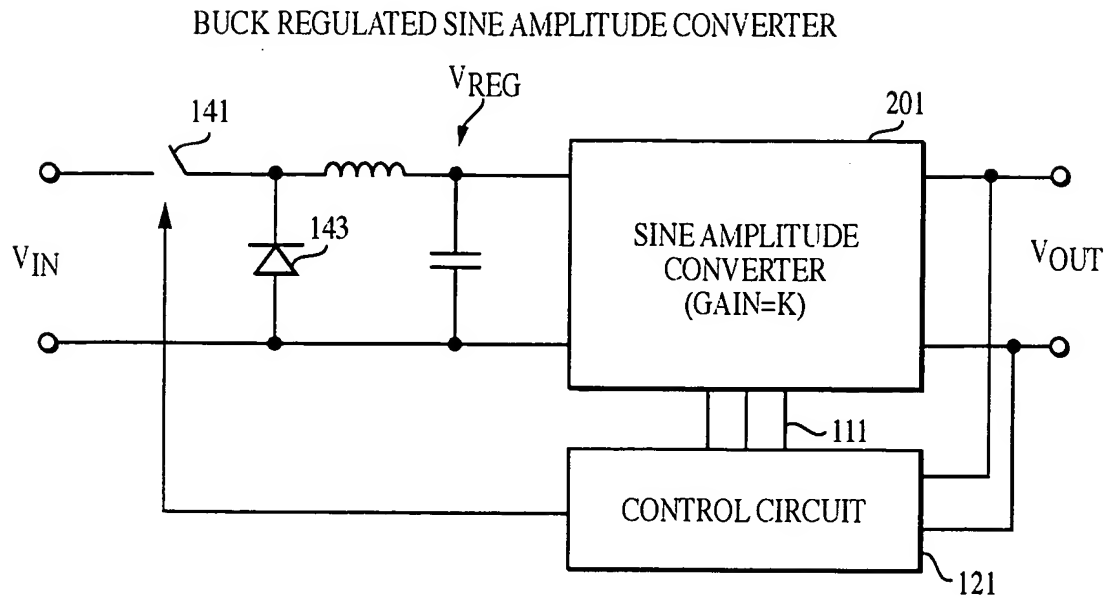


FIG. 29A

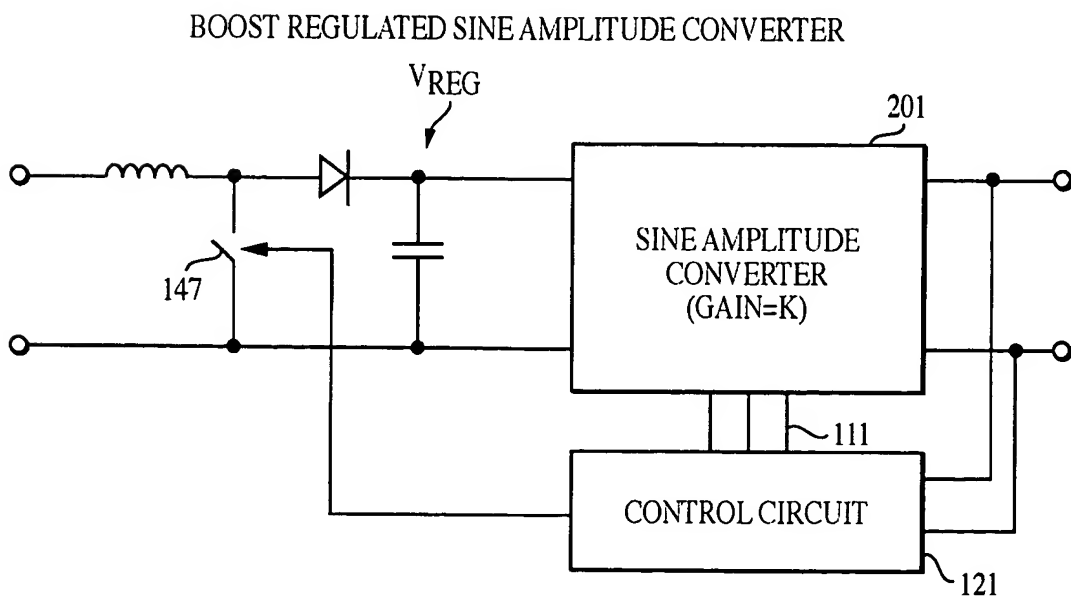


FIG. 29B

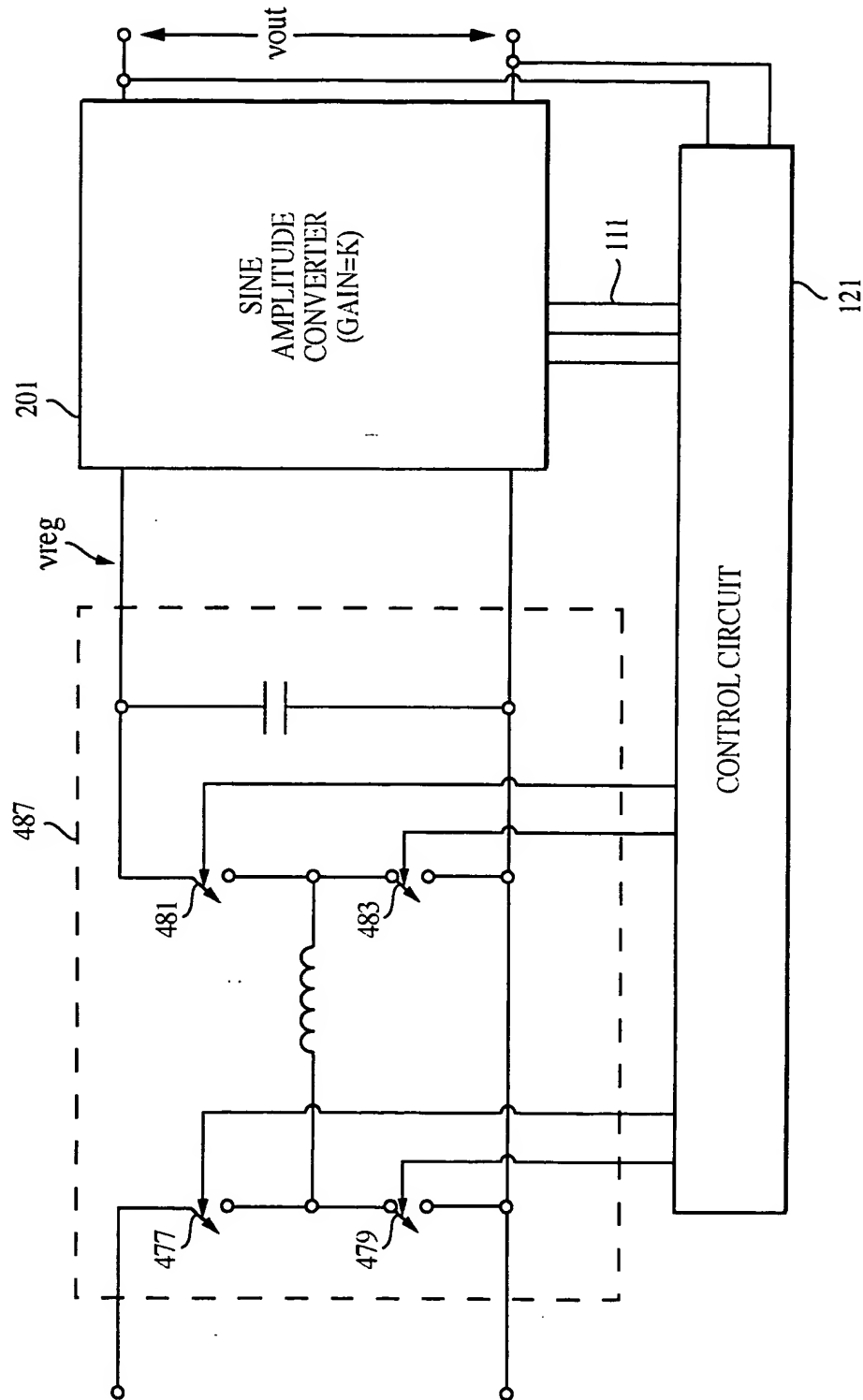


FIG. 29C

## BOOT STRAP REGULATED DC-DC CONVERTER

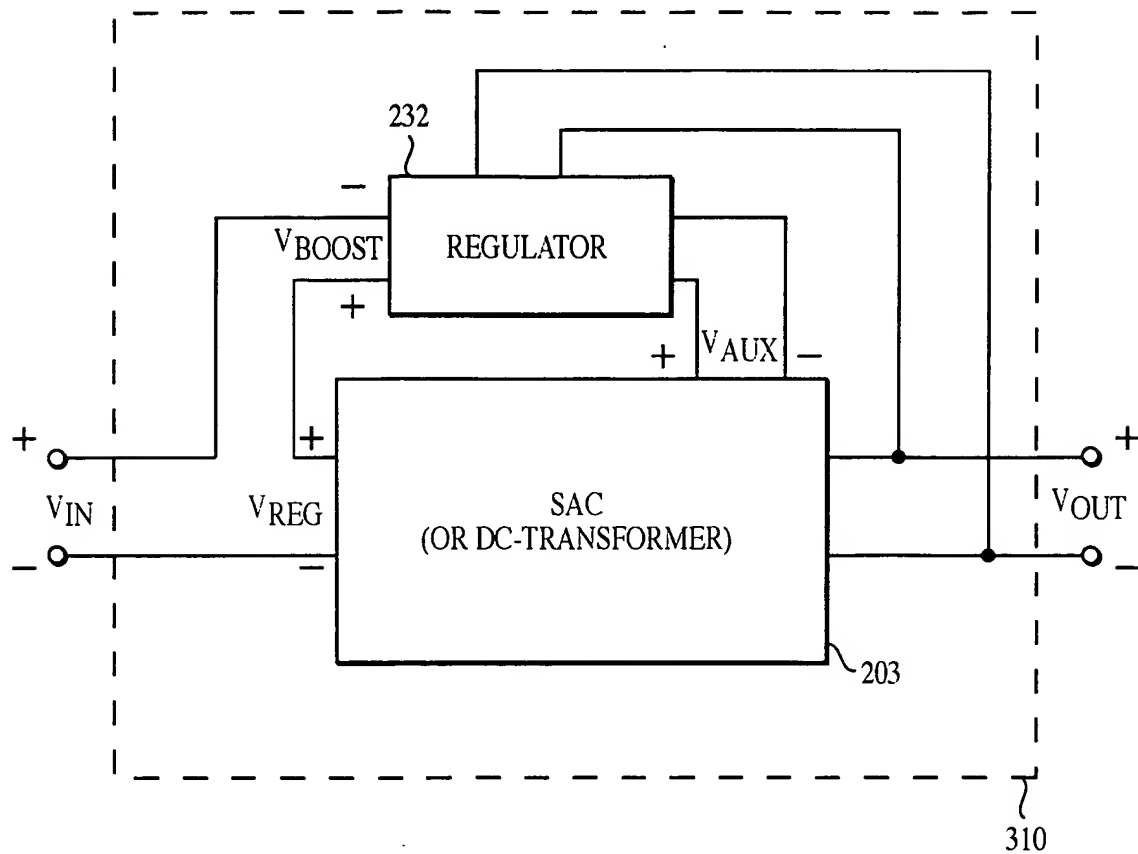


FIG. 30

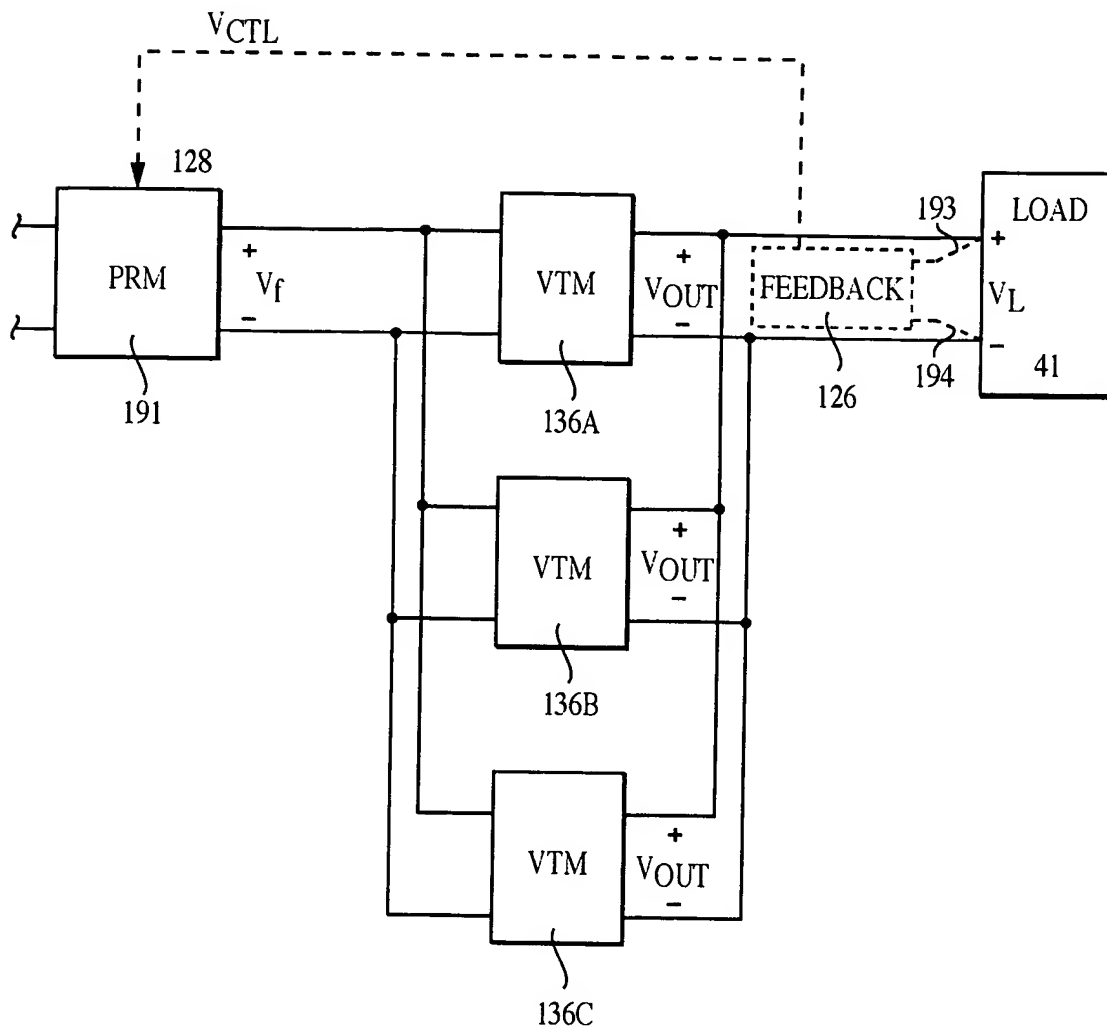


FIG. 31

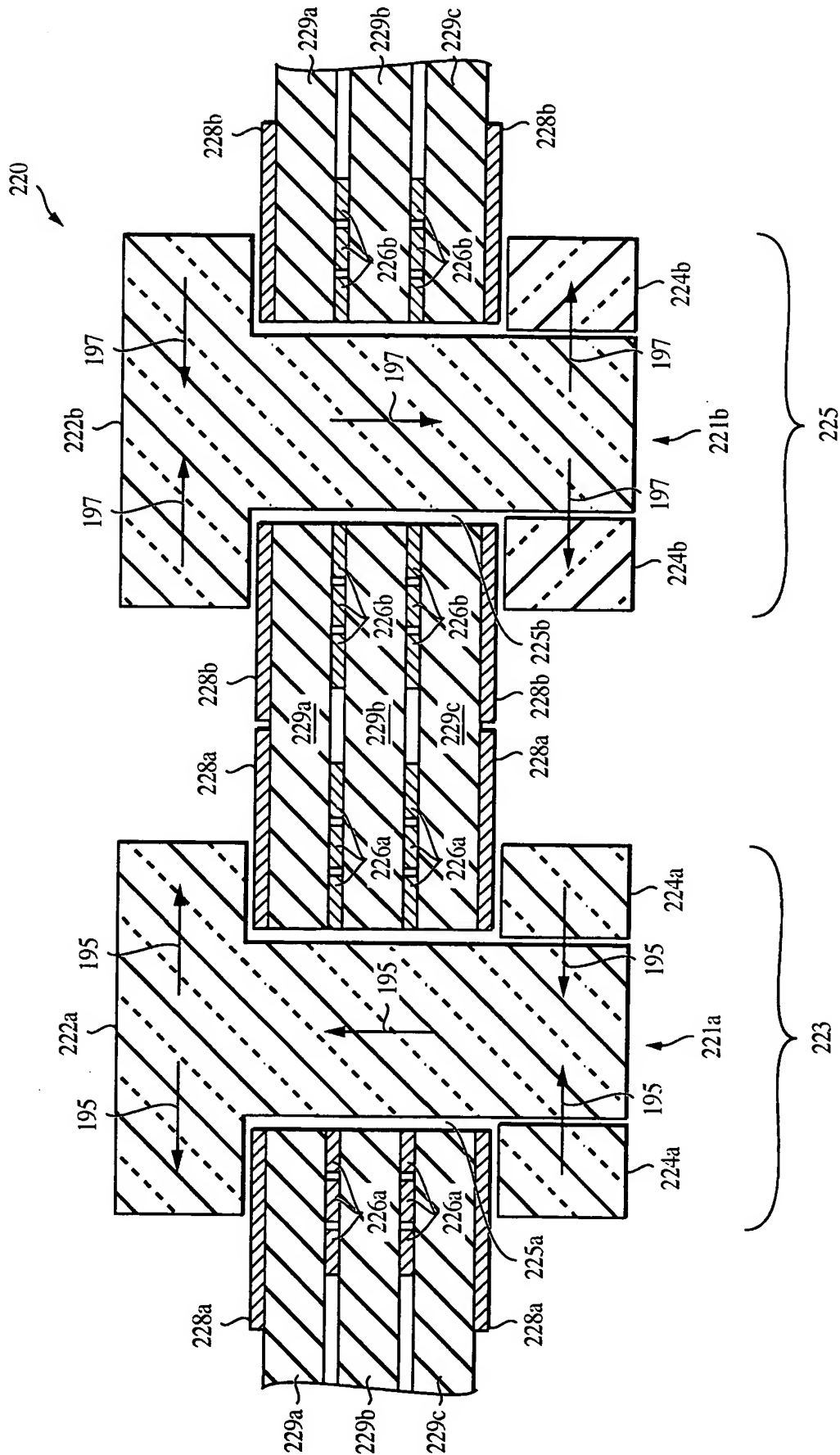


FIG. 32



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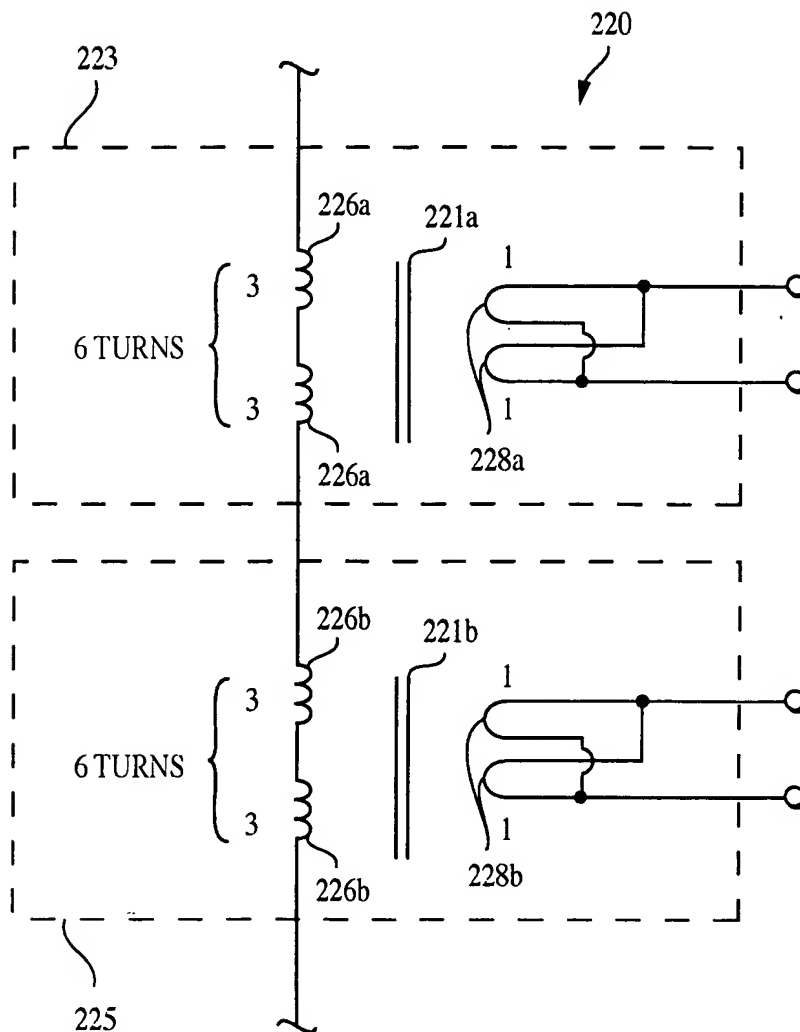
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FIG. 33

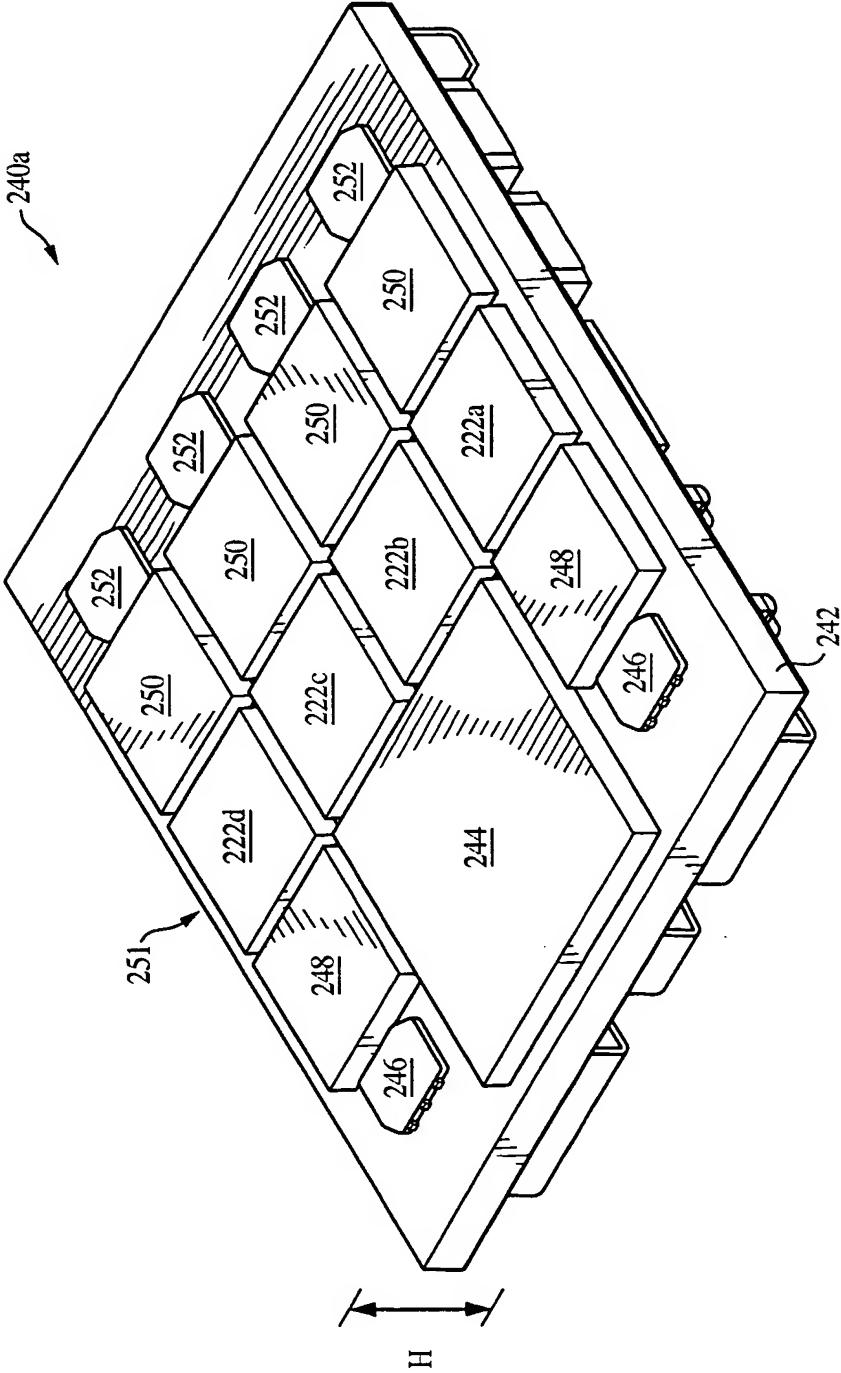
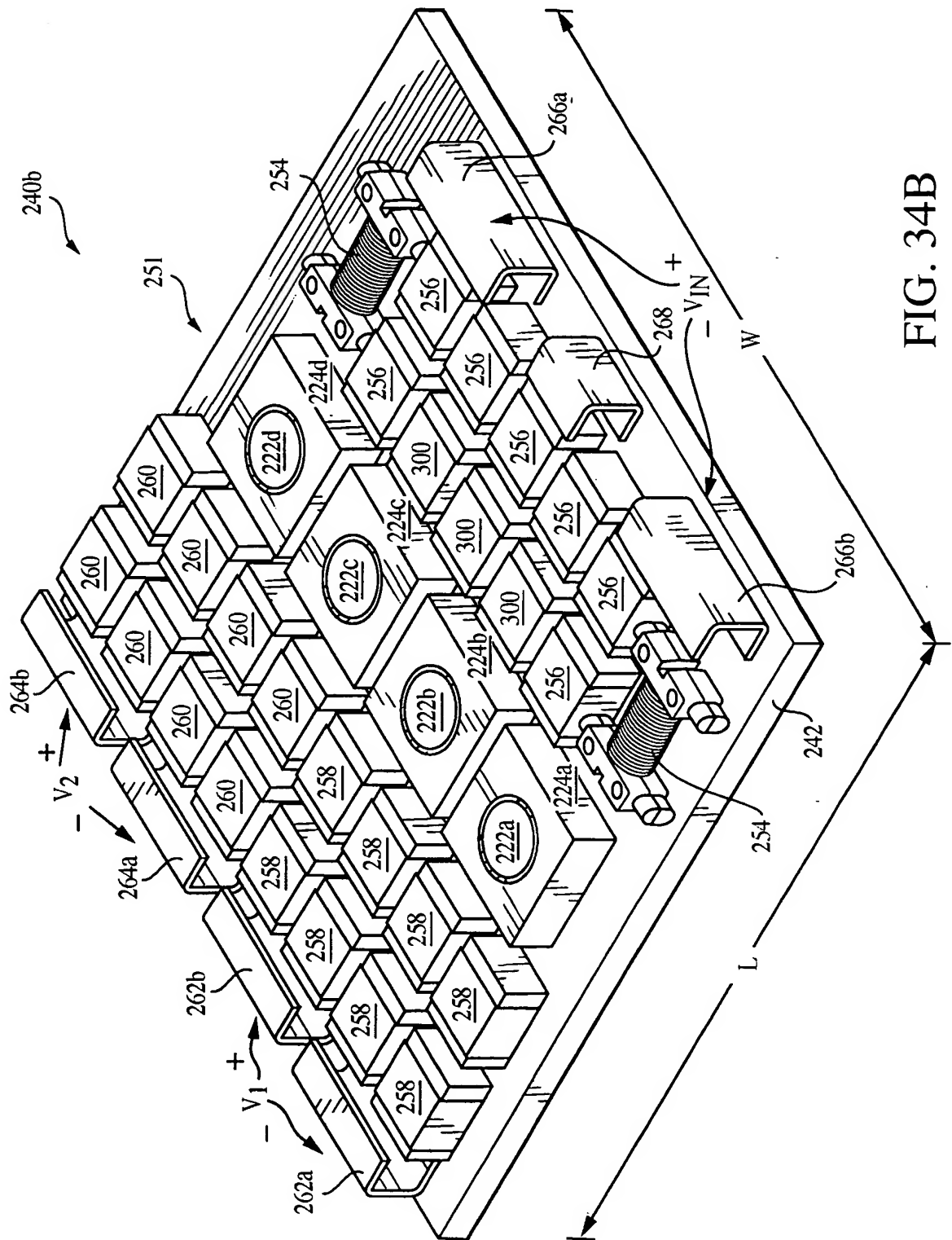


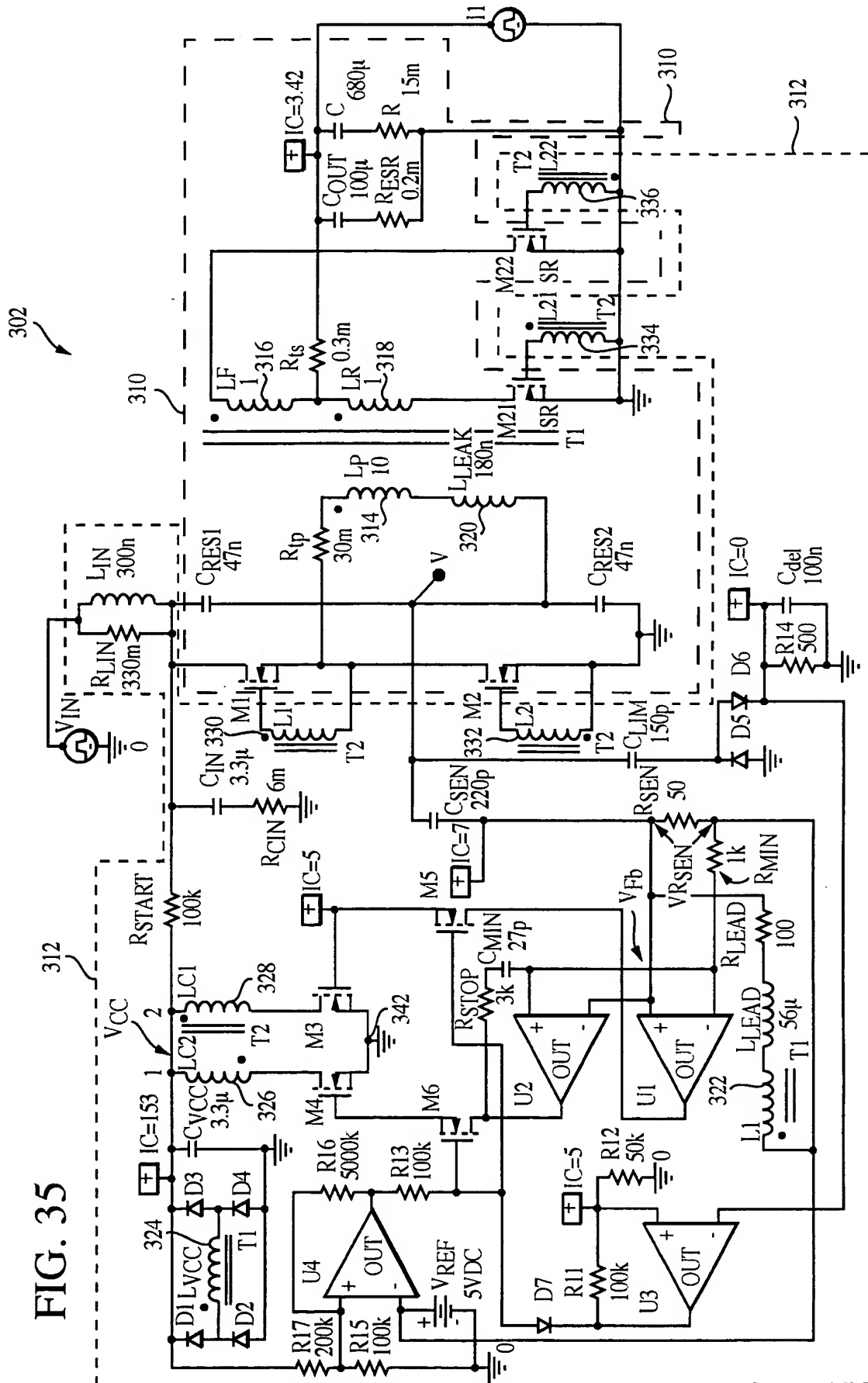
FIG. 34A

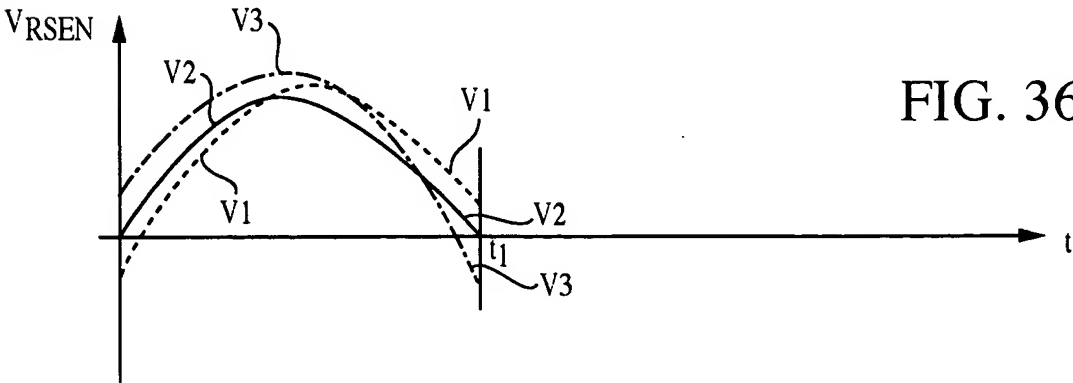
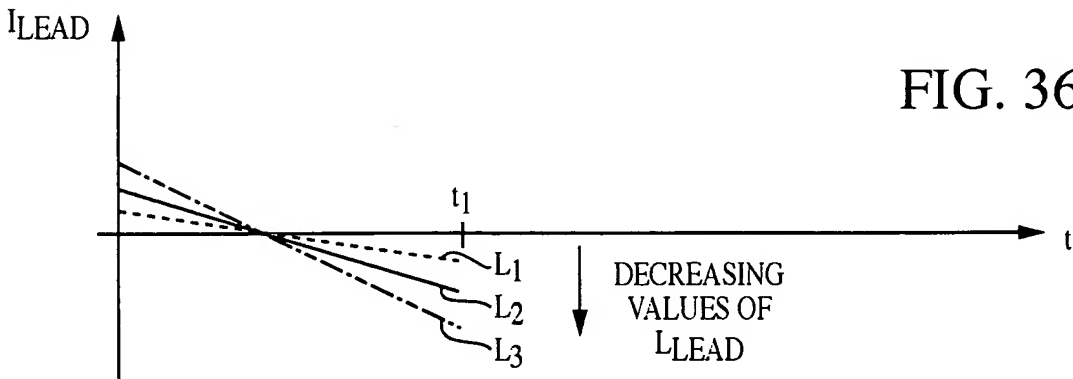
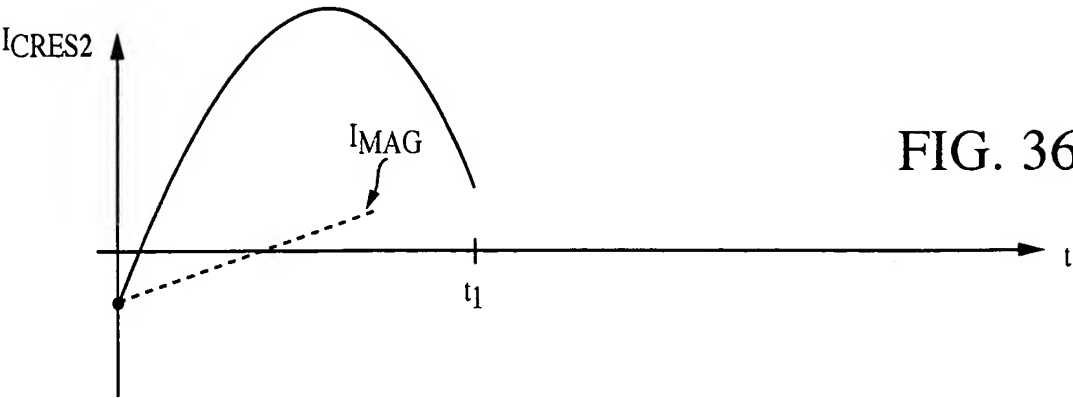
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LOAD SINE AMPLITUDE CONVERTERS

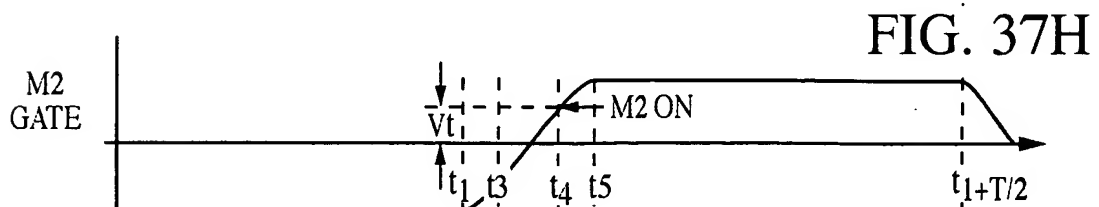
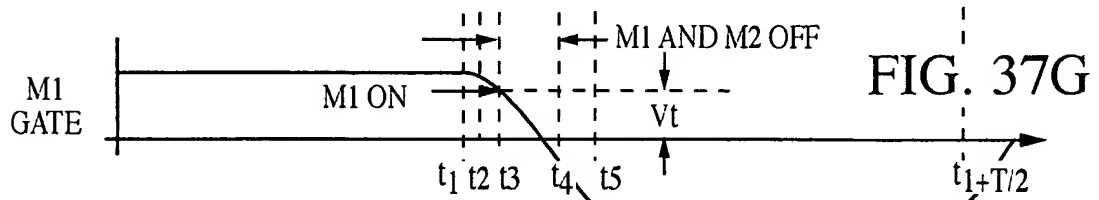
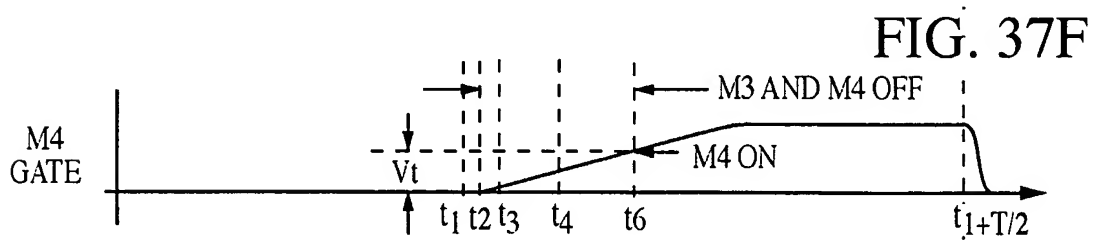
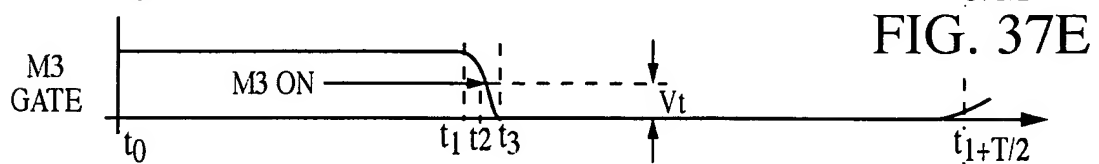
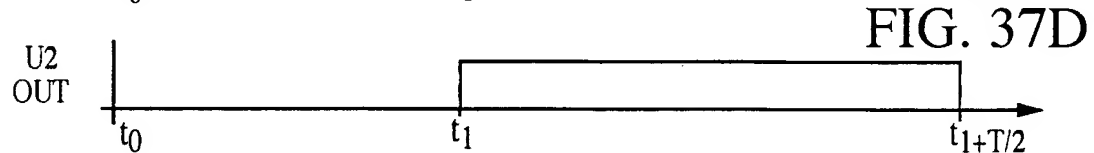
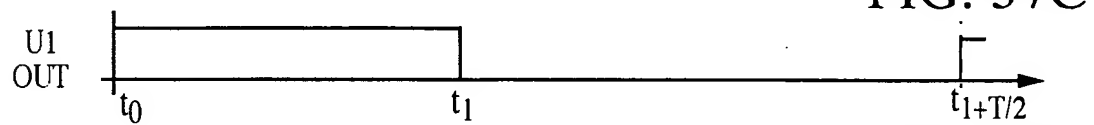
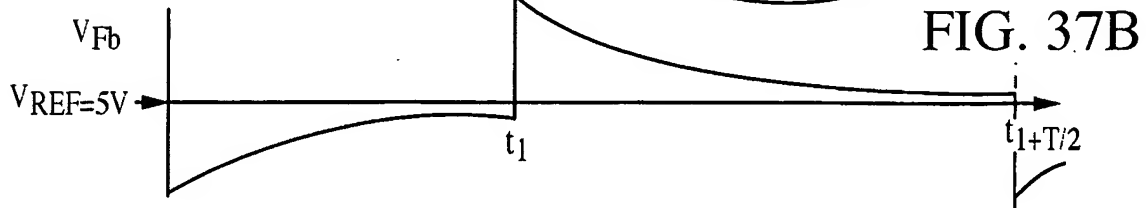
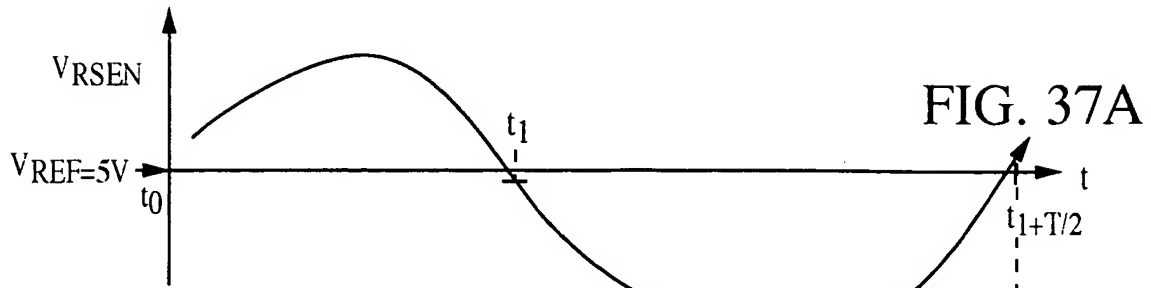


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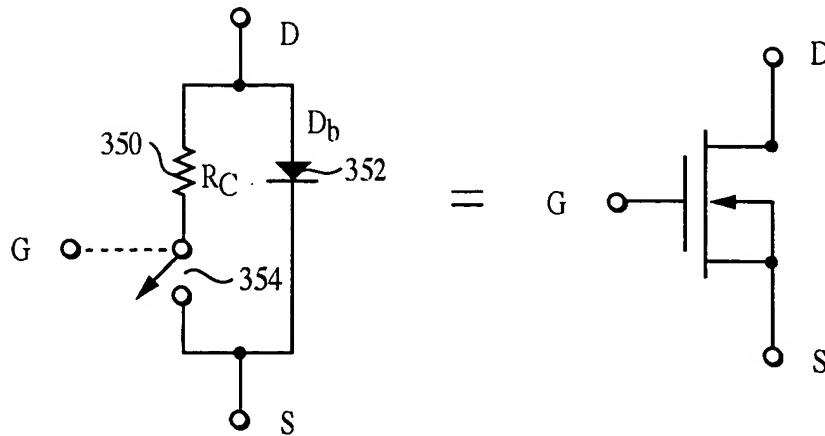


FIG. 38

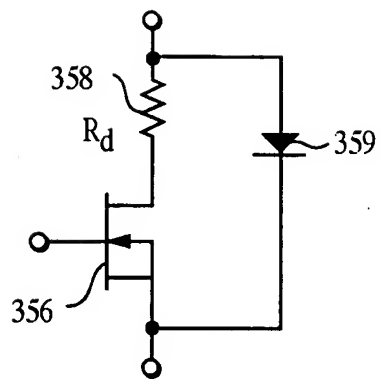


FIG. 39A

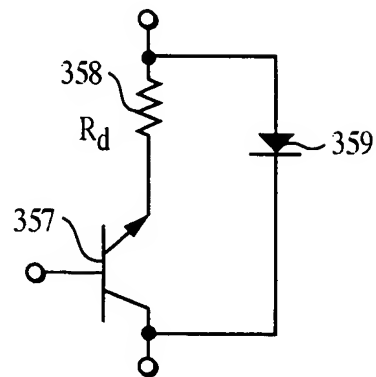


FIG. 39B

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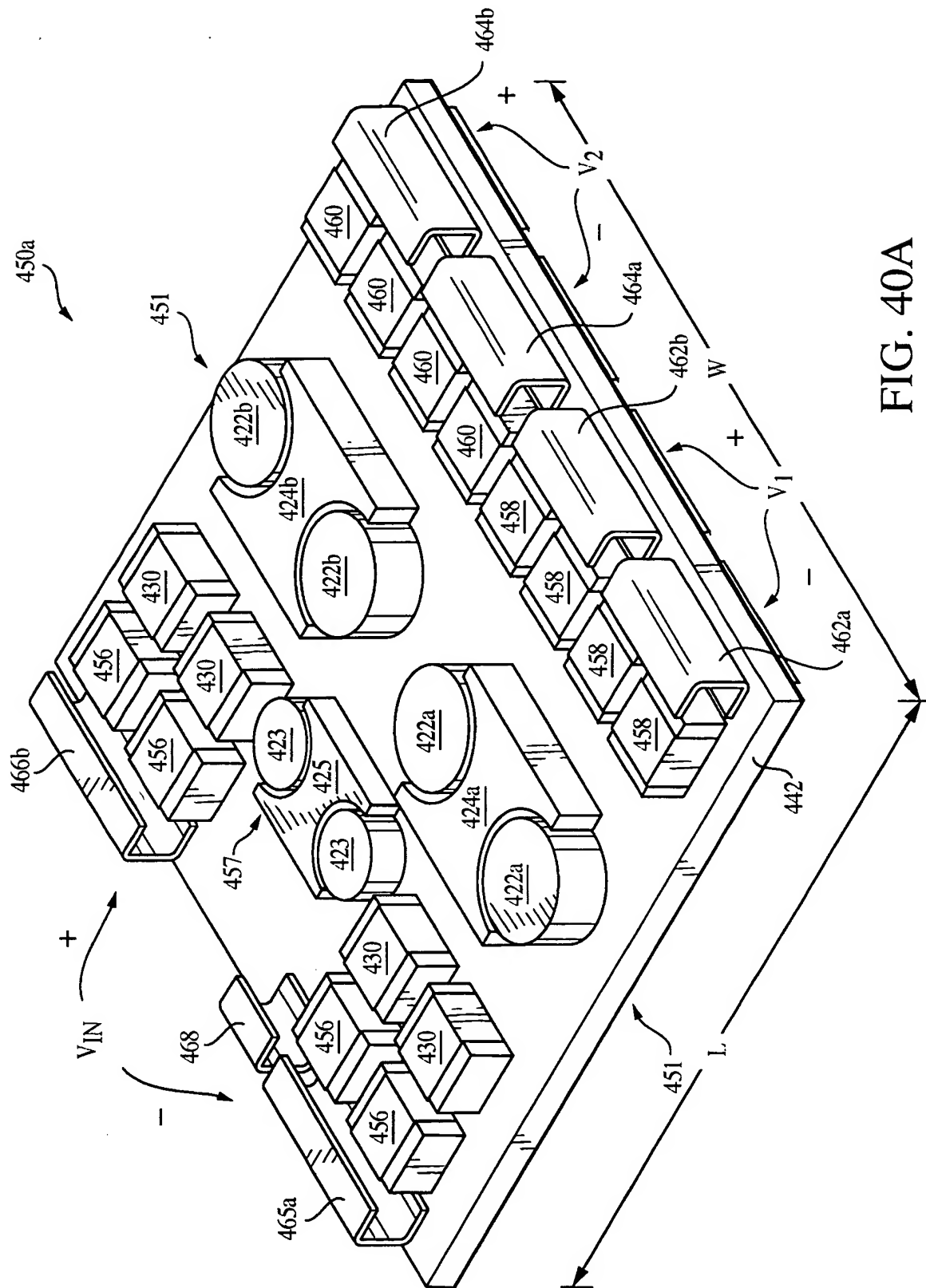
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FIG. 40A



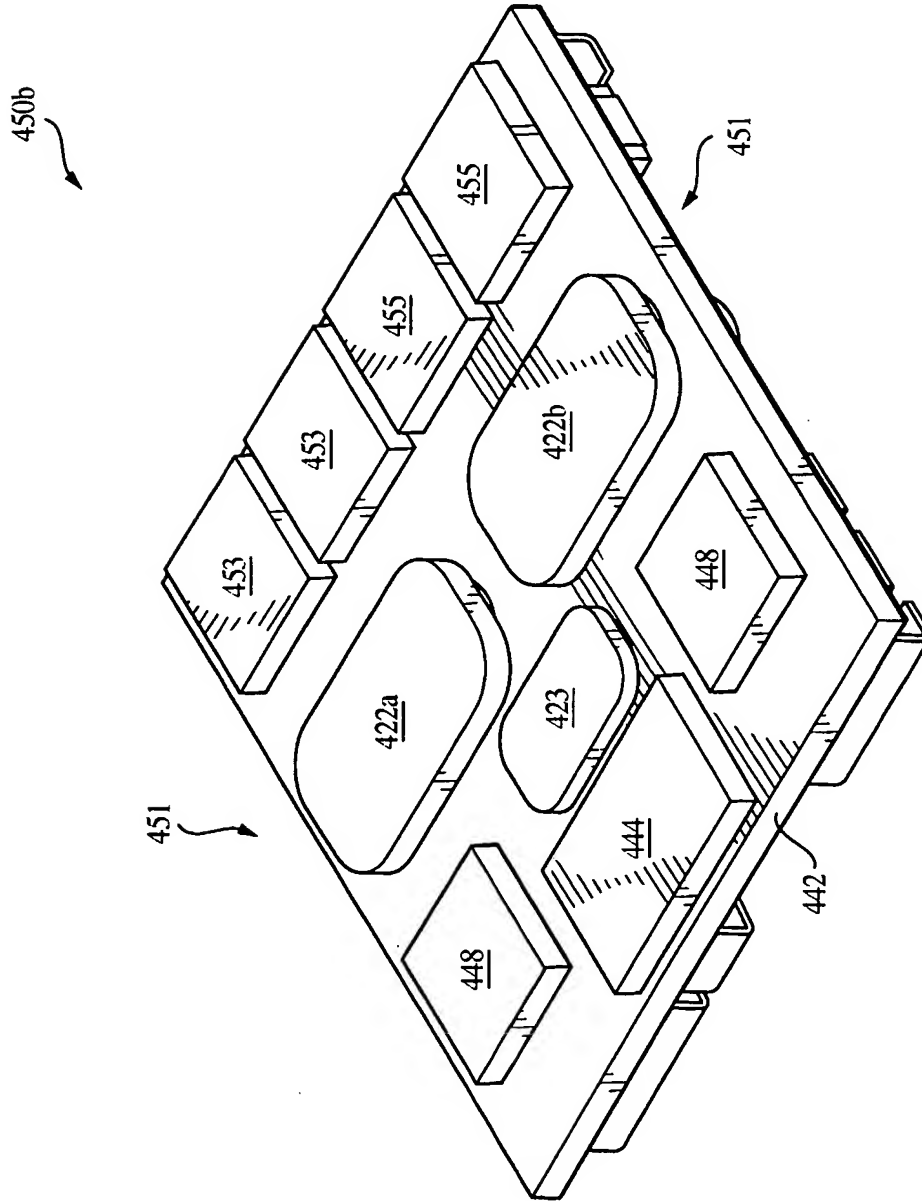


FIG. 40B

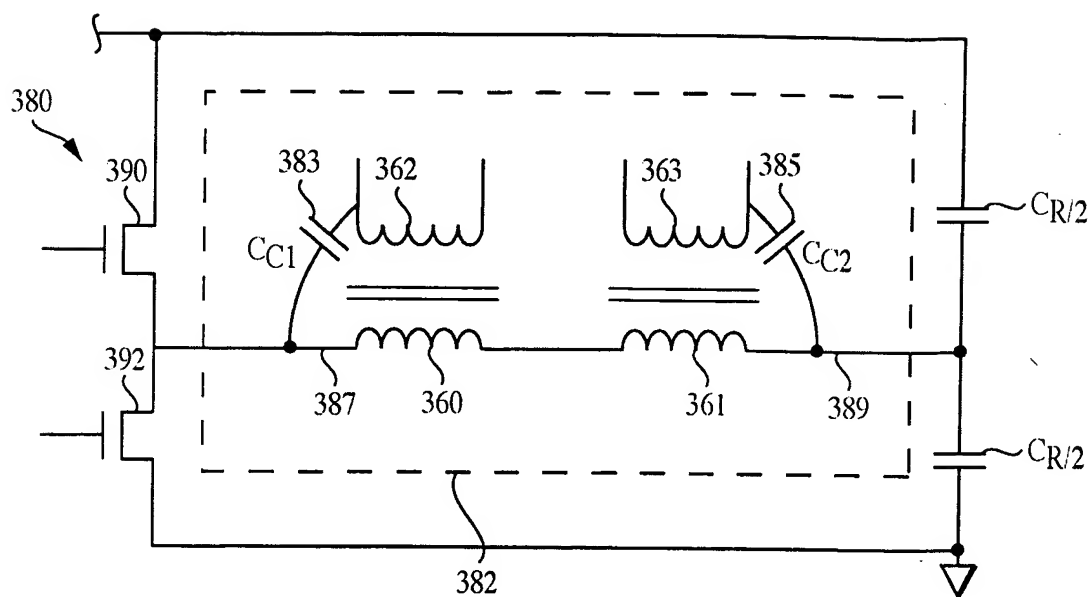


FIG. 41

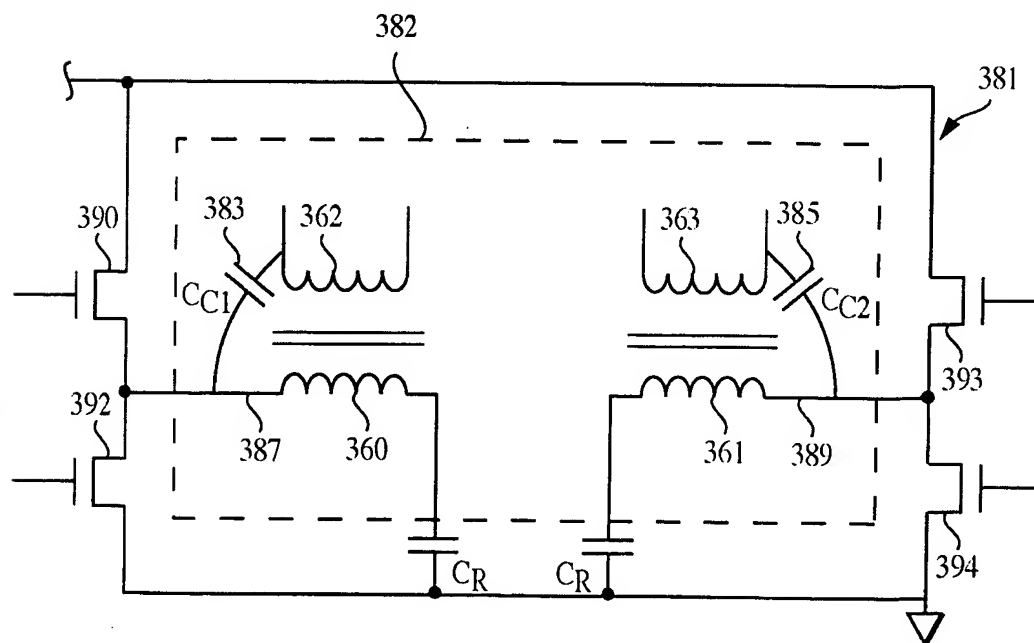


FIG. 42

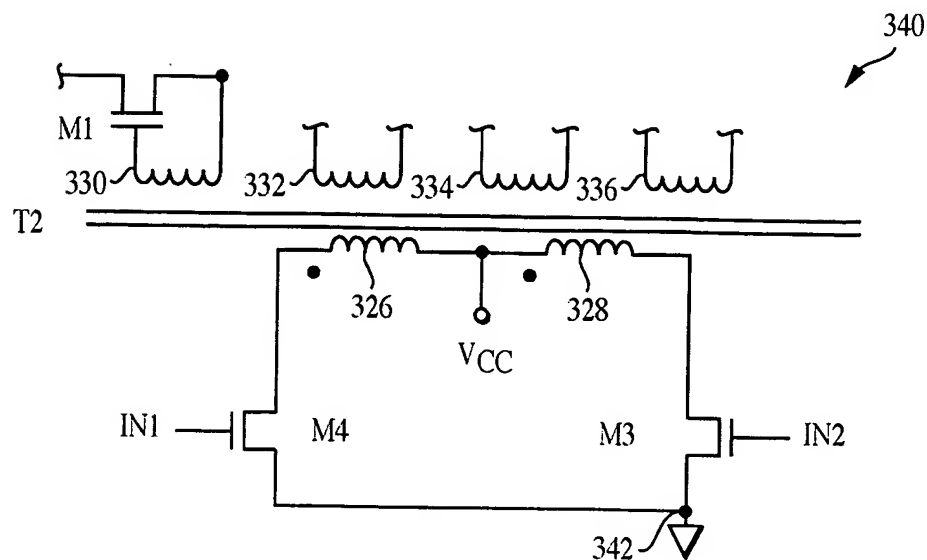


FIG. 43

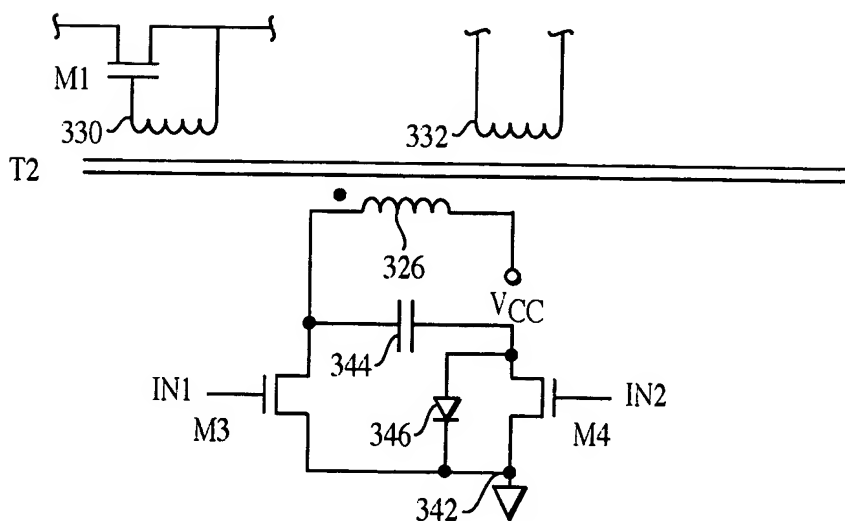


FIG. 44

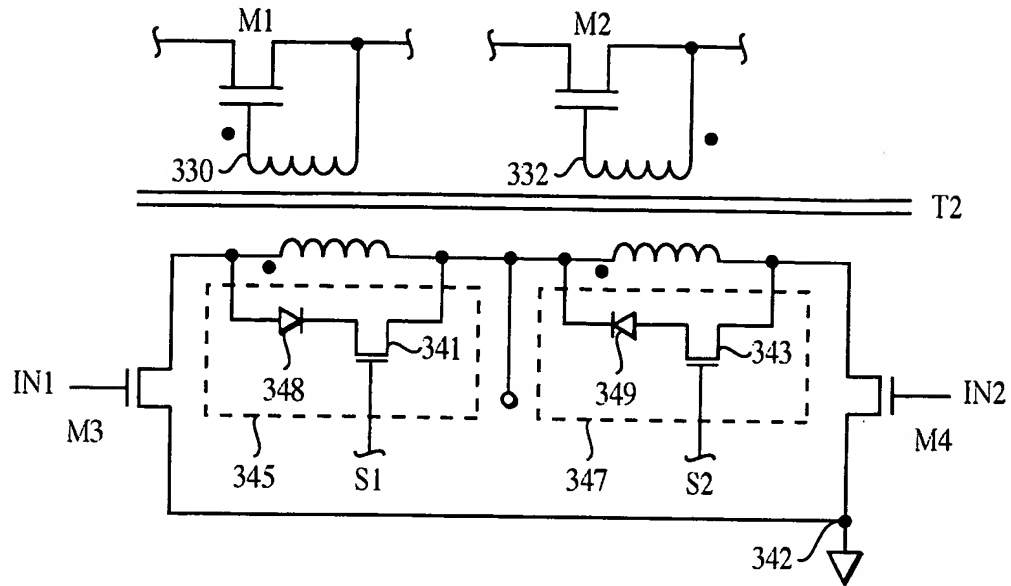


FIG. 45

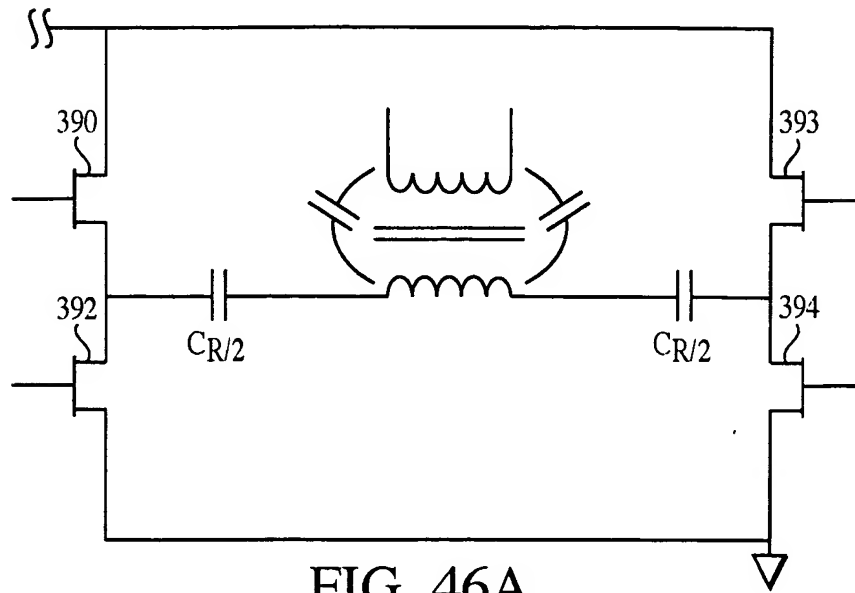


FIG. 46A

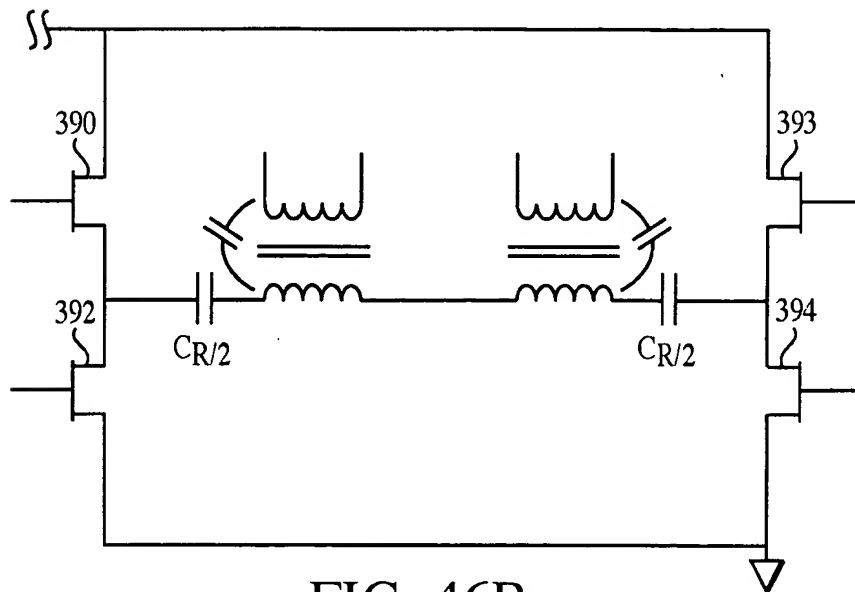


FIG. 46B

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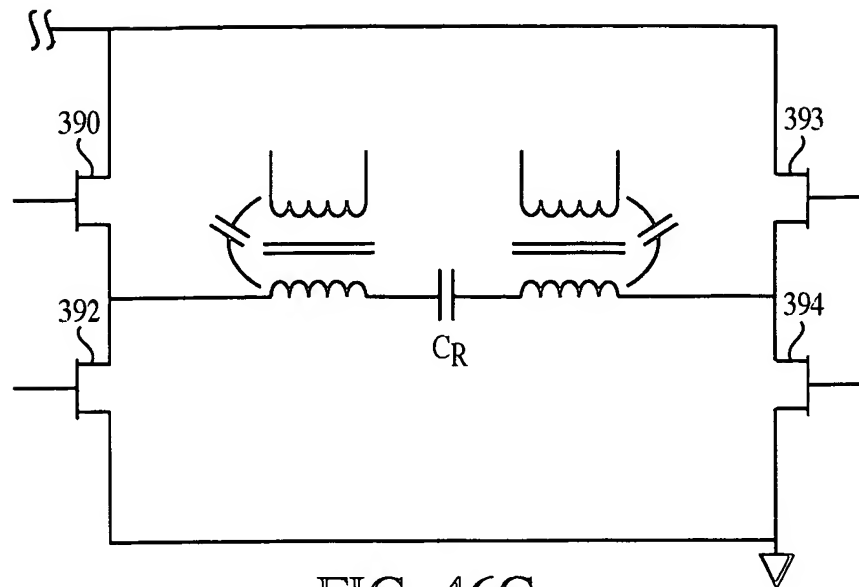
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FIG. 46C

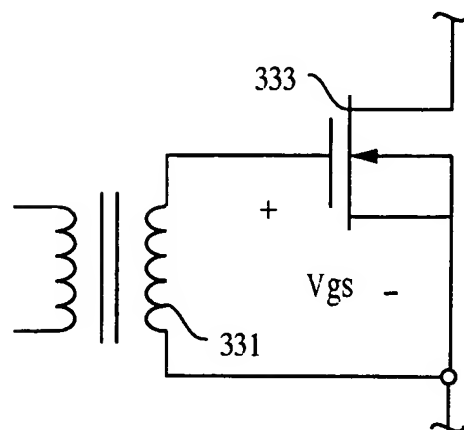


FIG. 47A

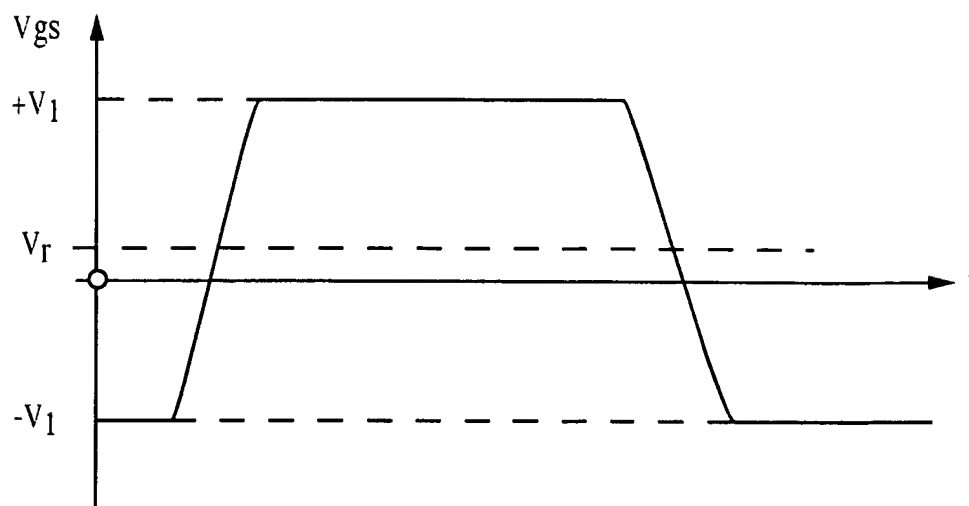


FIG. 47B

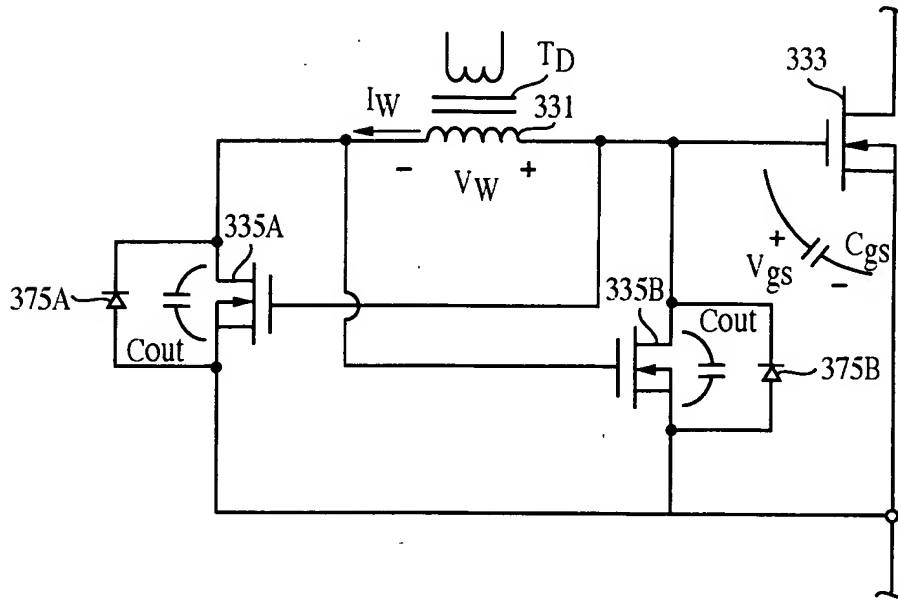
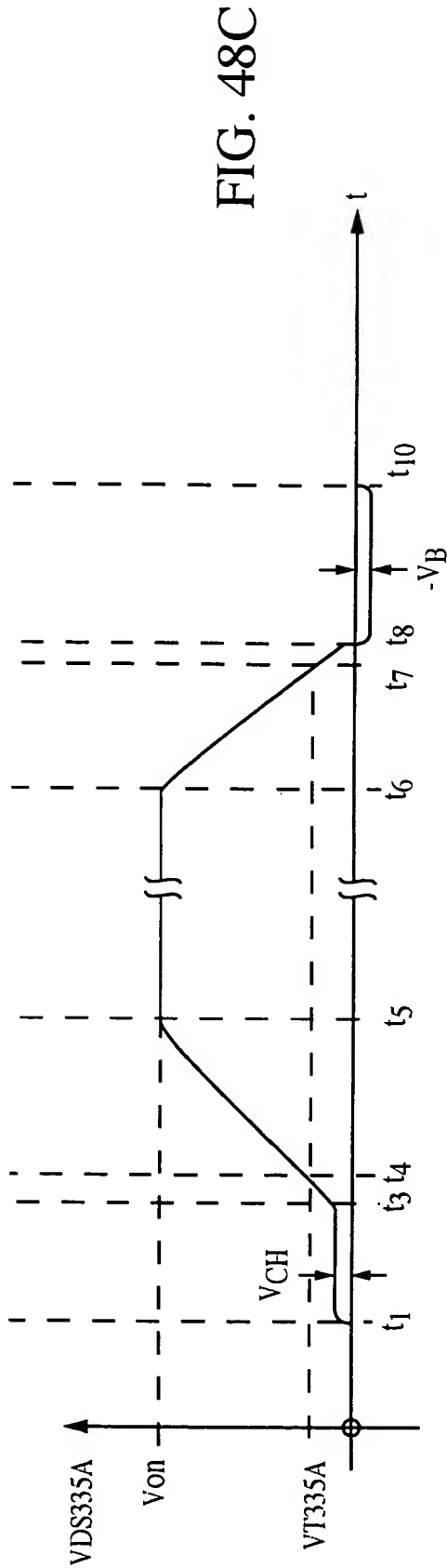
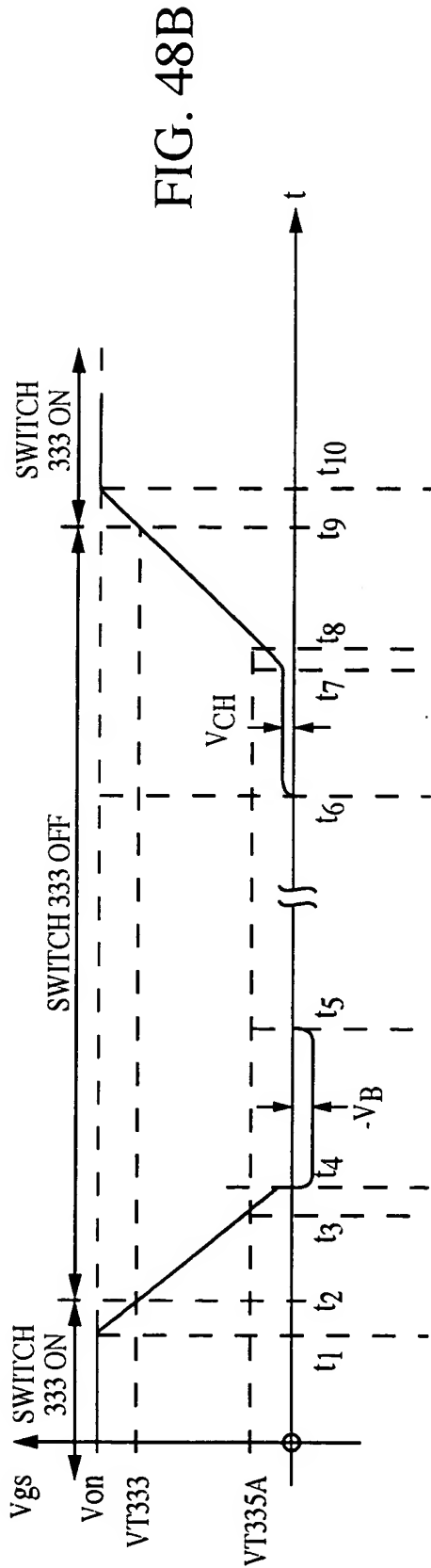


FIG. 48A





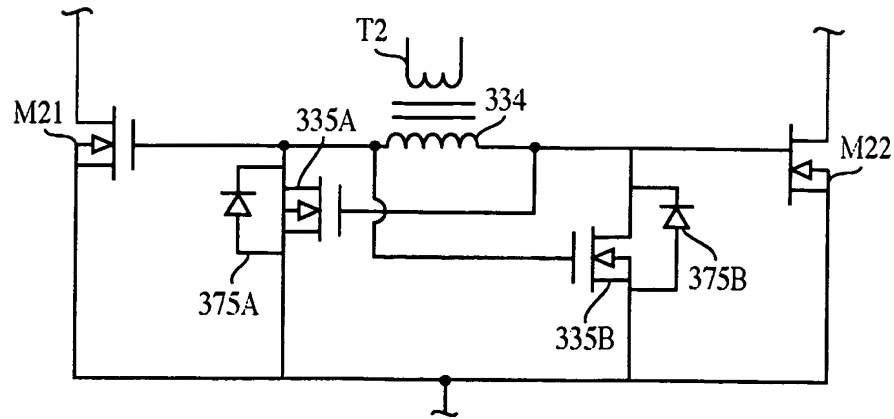


FIG. 49

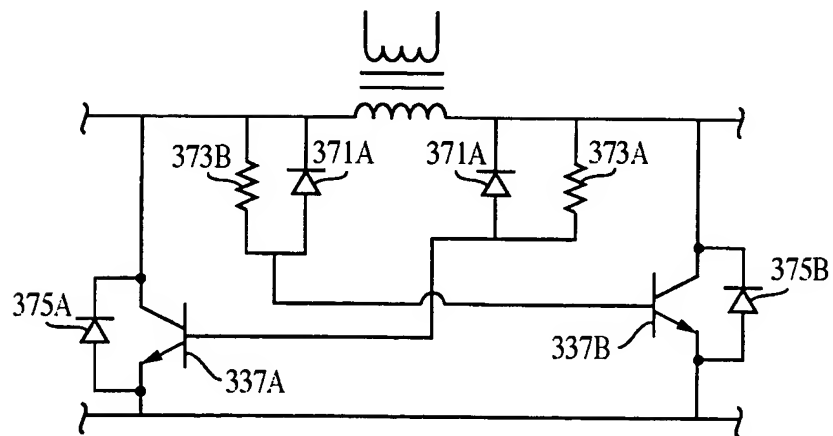


FIG. 50

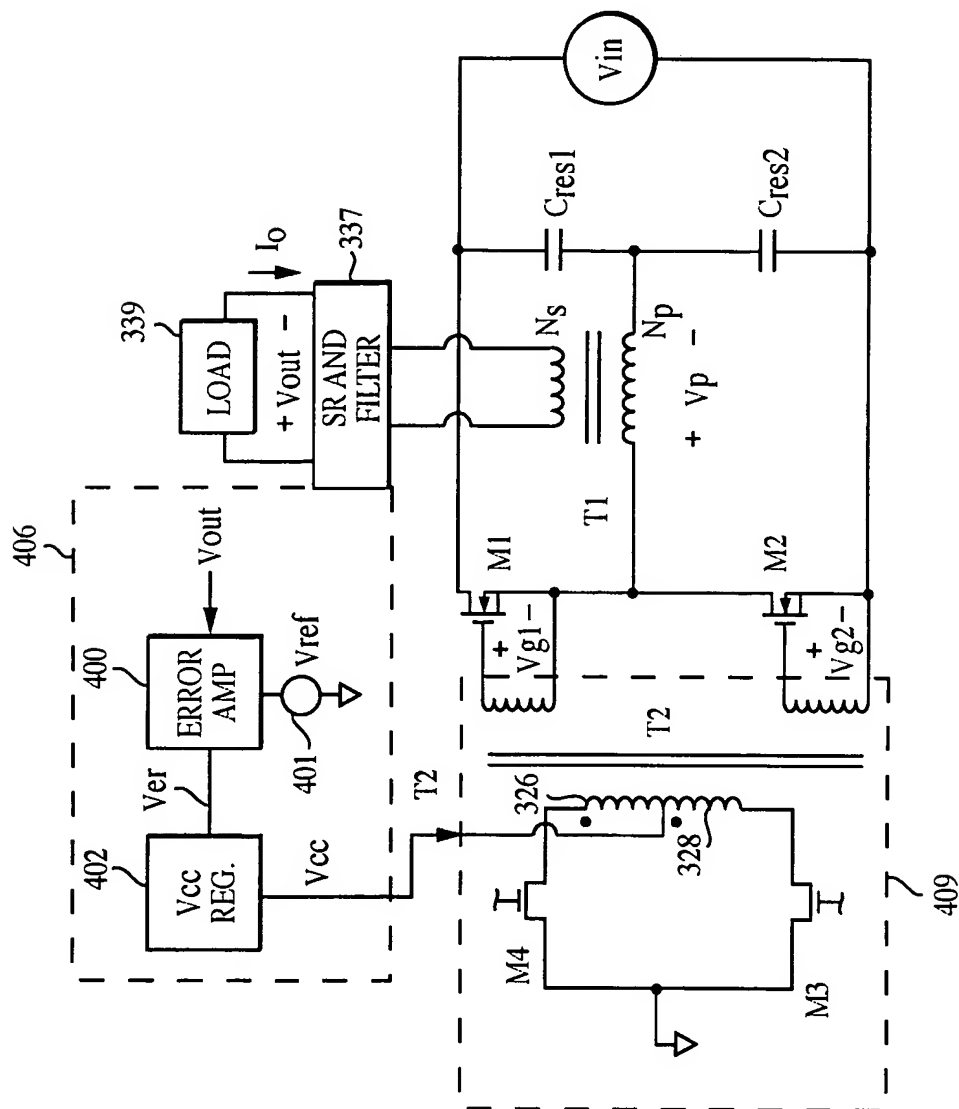


FIG. 51

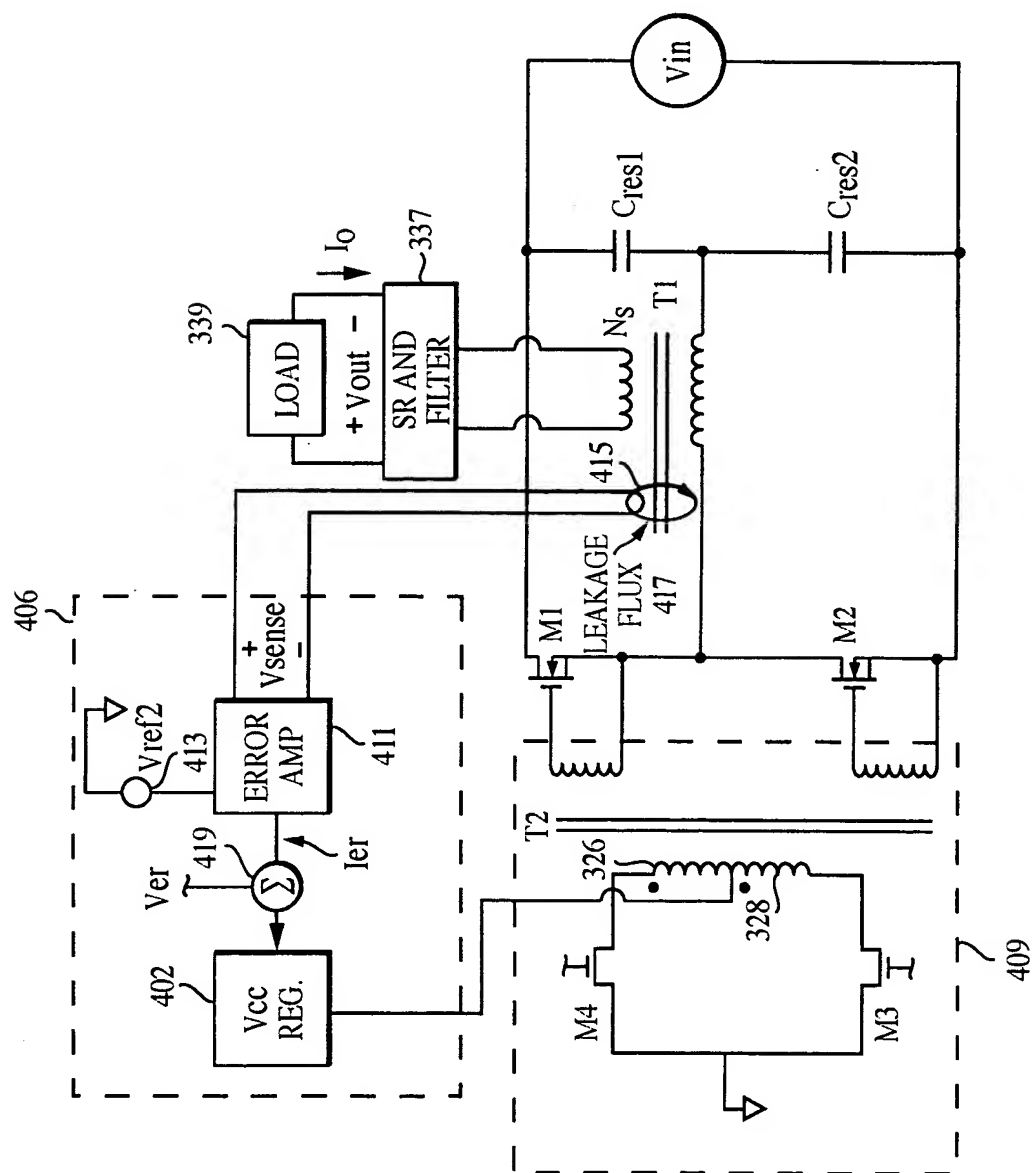


FIG. 52

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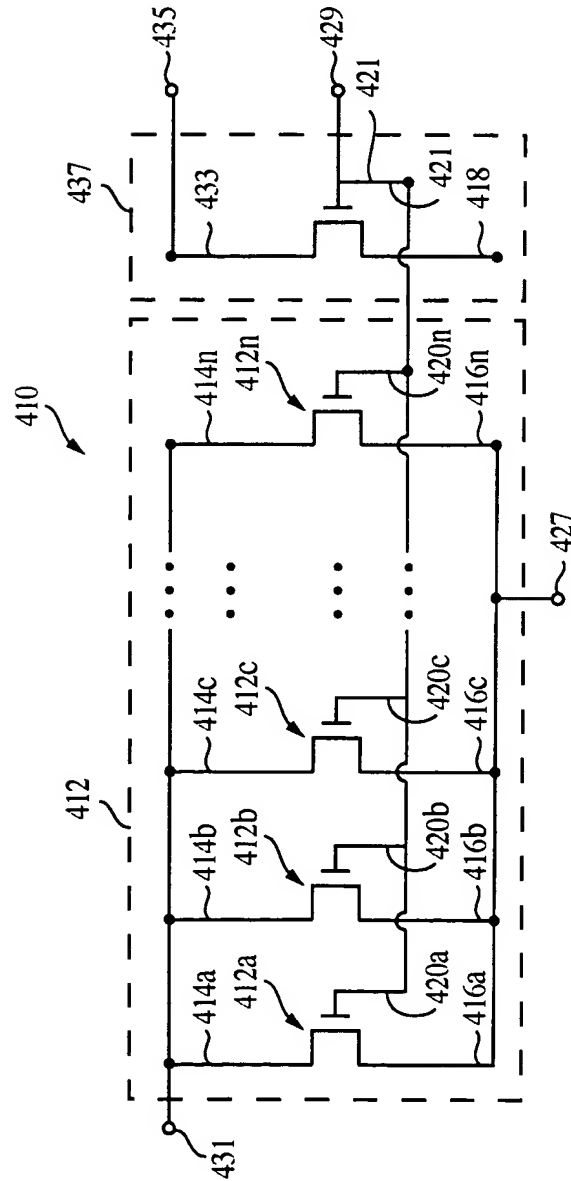
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FIG. 53

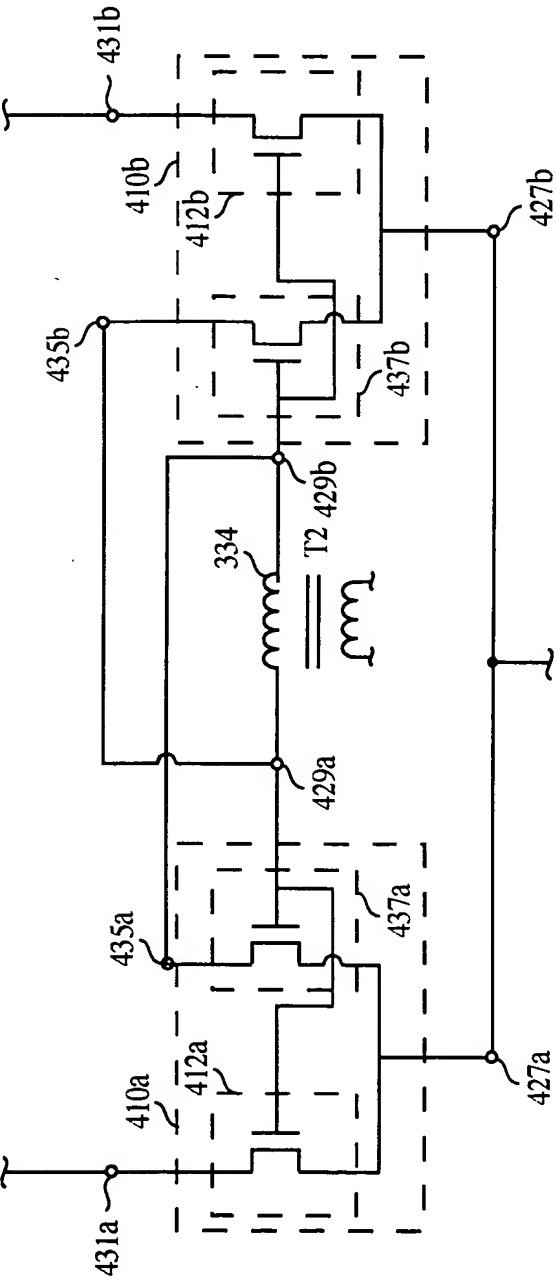


FIG. 54

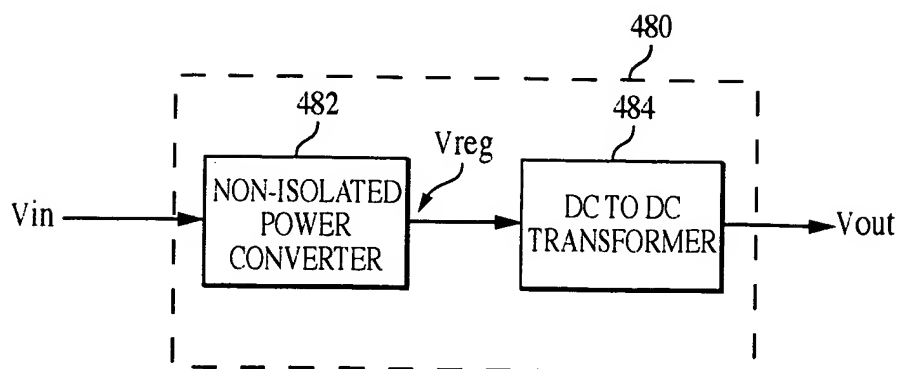


FIG. 55A

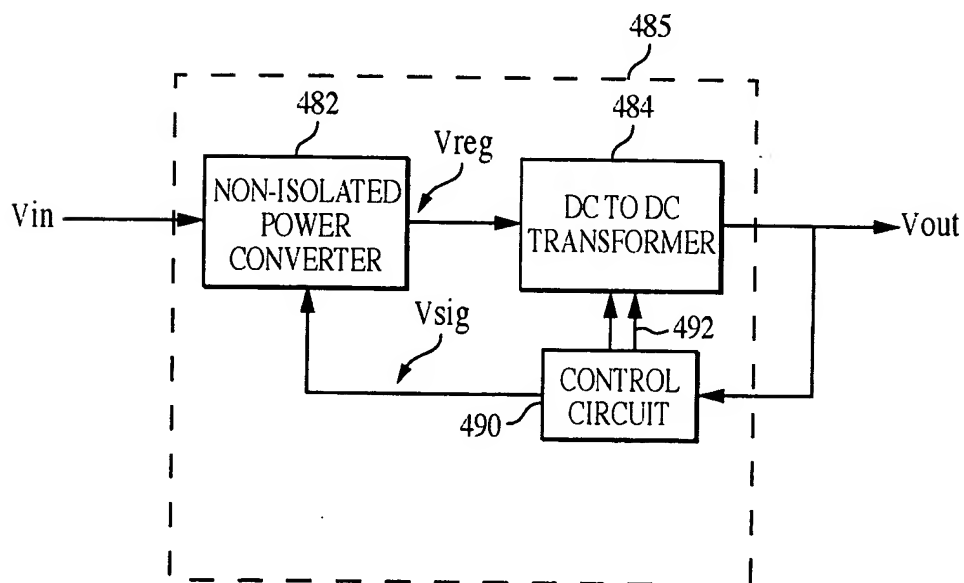


FIG. 55B

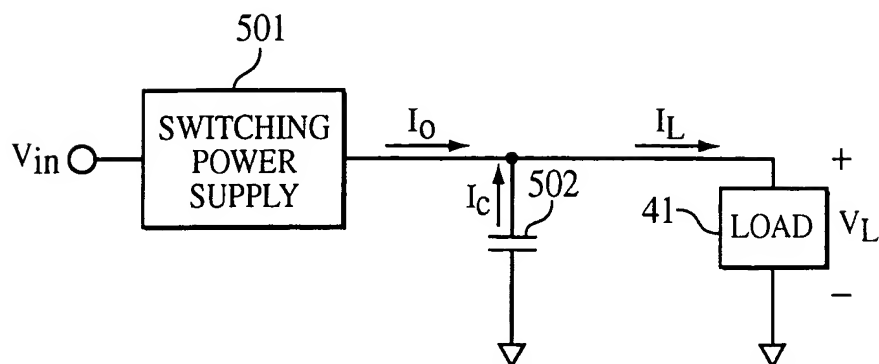


FIG. 56

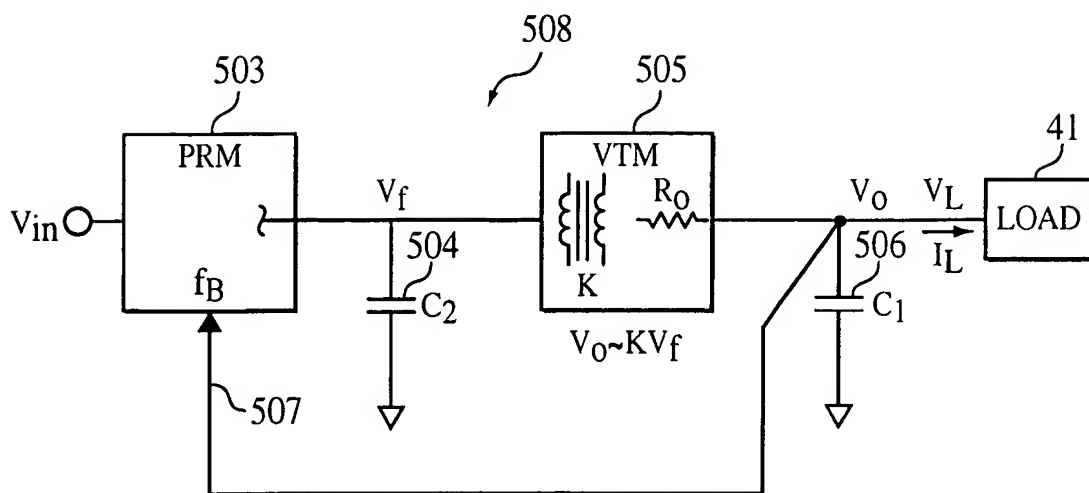


FIG. 58



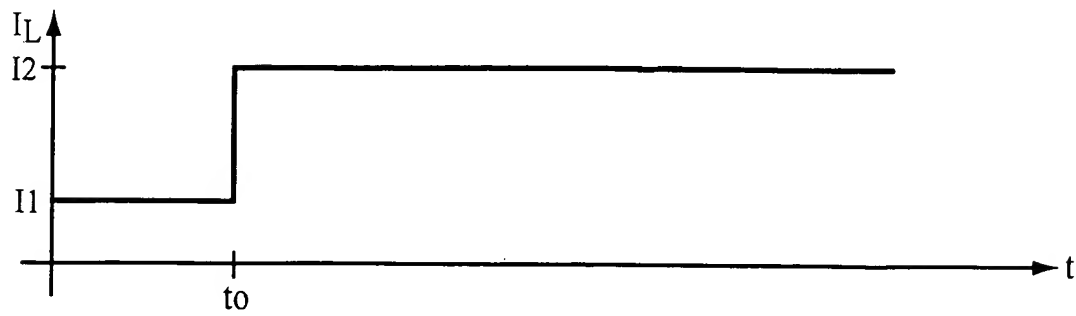


FIG. 57A

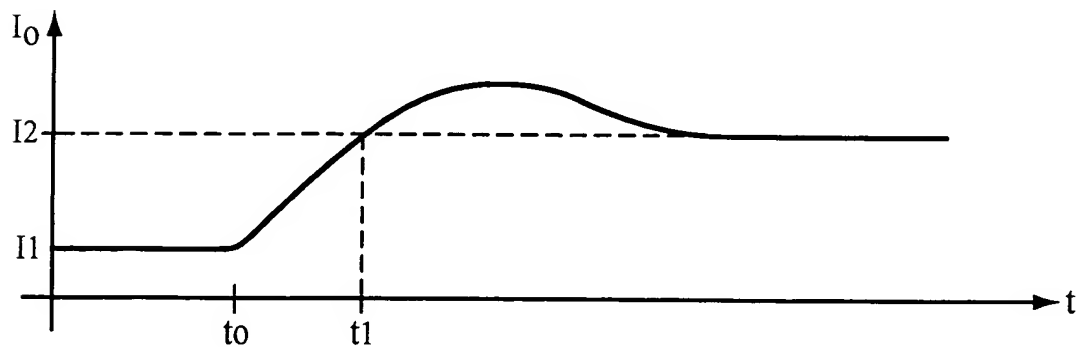


FIG. 57B

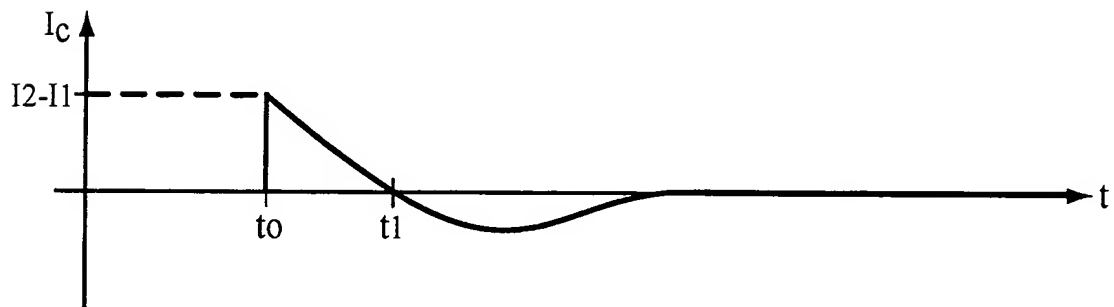


FIG. 57C

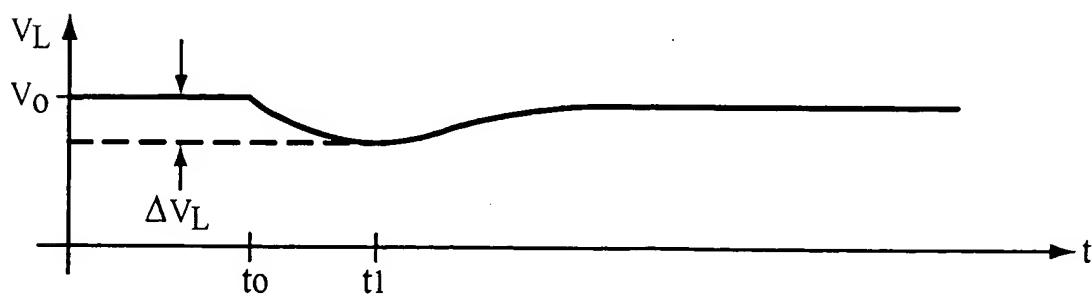


FIG. 57D

Applicant(s): Patrizio Vinciarelli

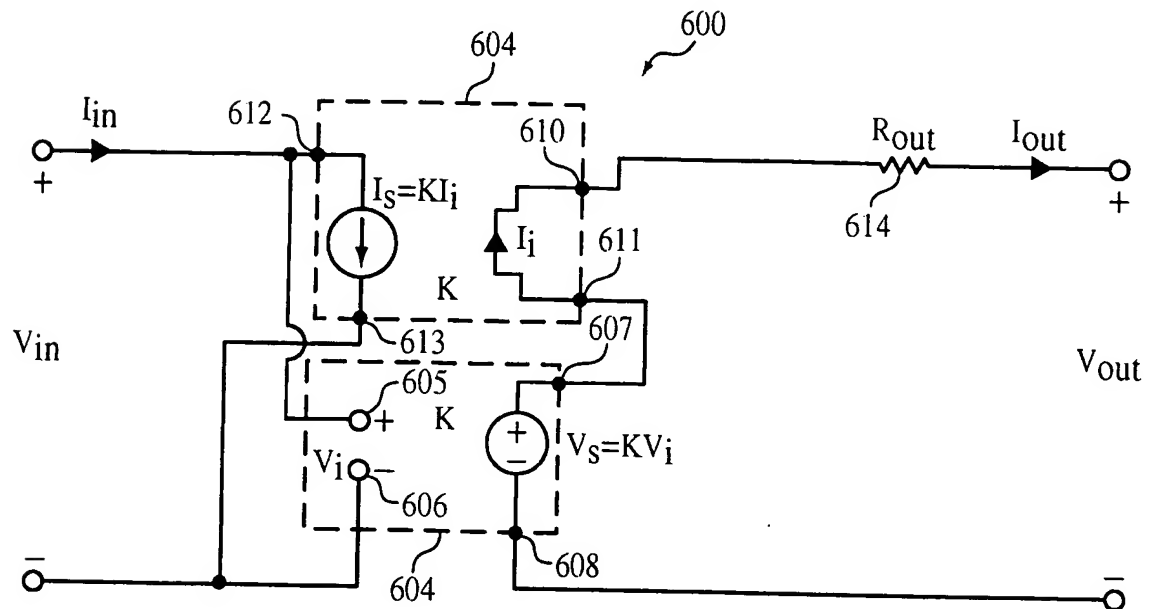
FACTORIZED POWER ARCHITECTURE WITH POINT OF  
LOAD SINE AMPLITUDE CONVERTERS

FIG. 59A

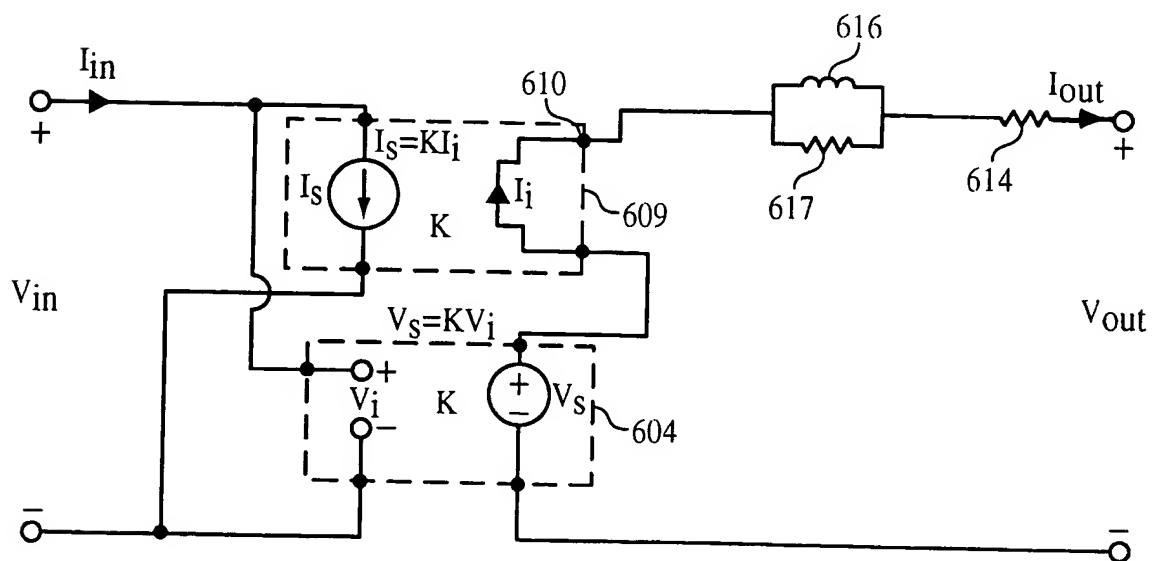


FIG. 59B

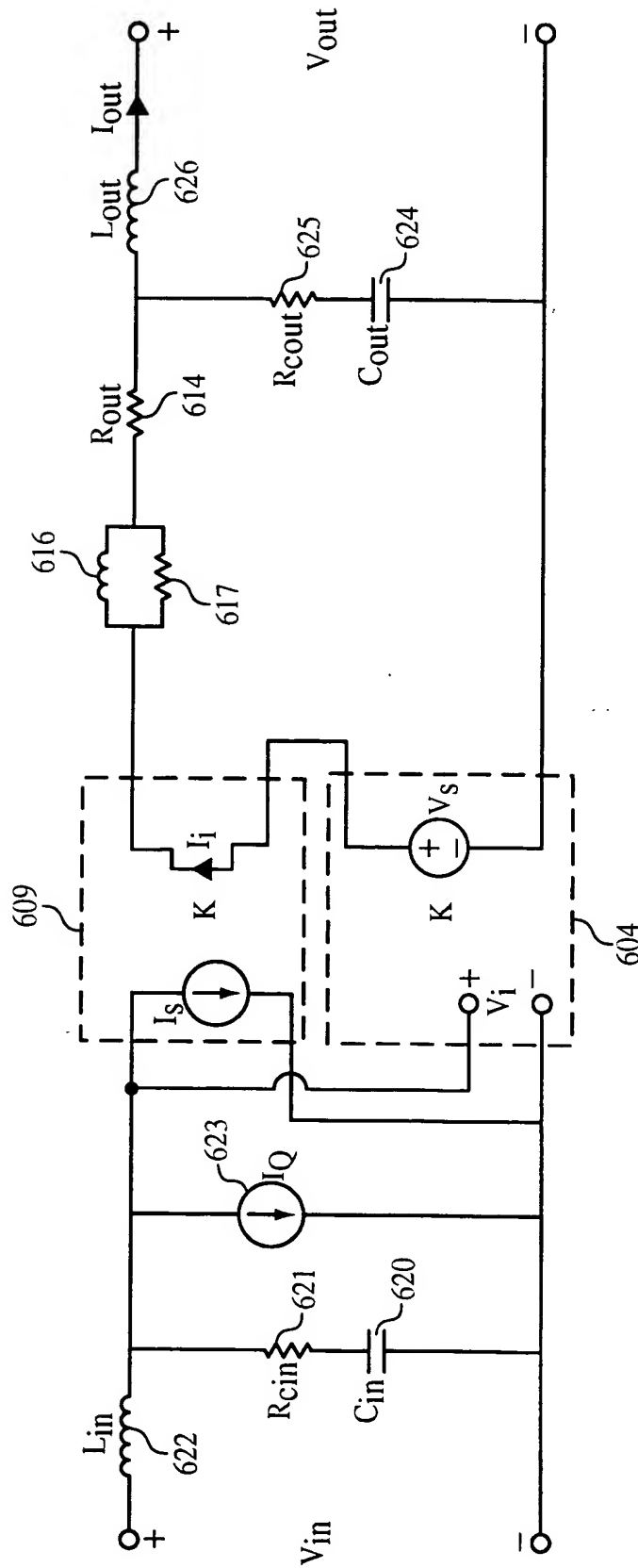


FIG. 59C